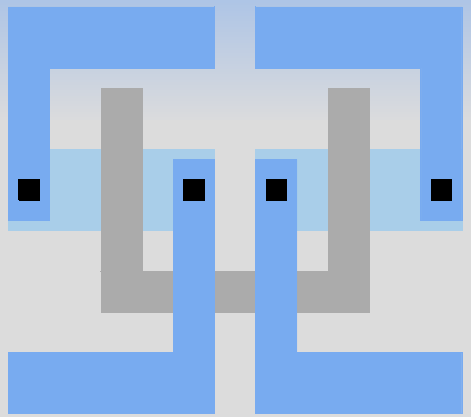
A Multi Channel ASIC for High Resolution Time Measurements



Schaltungstechnik und Simulation

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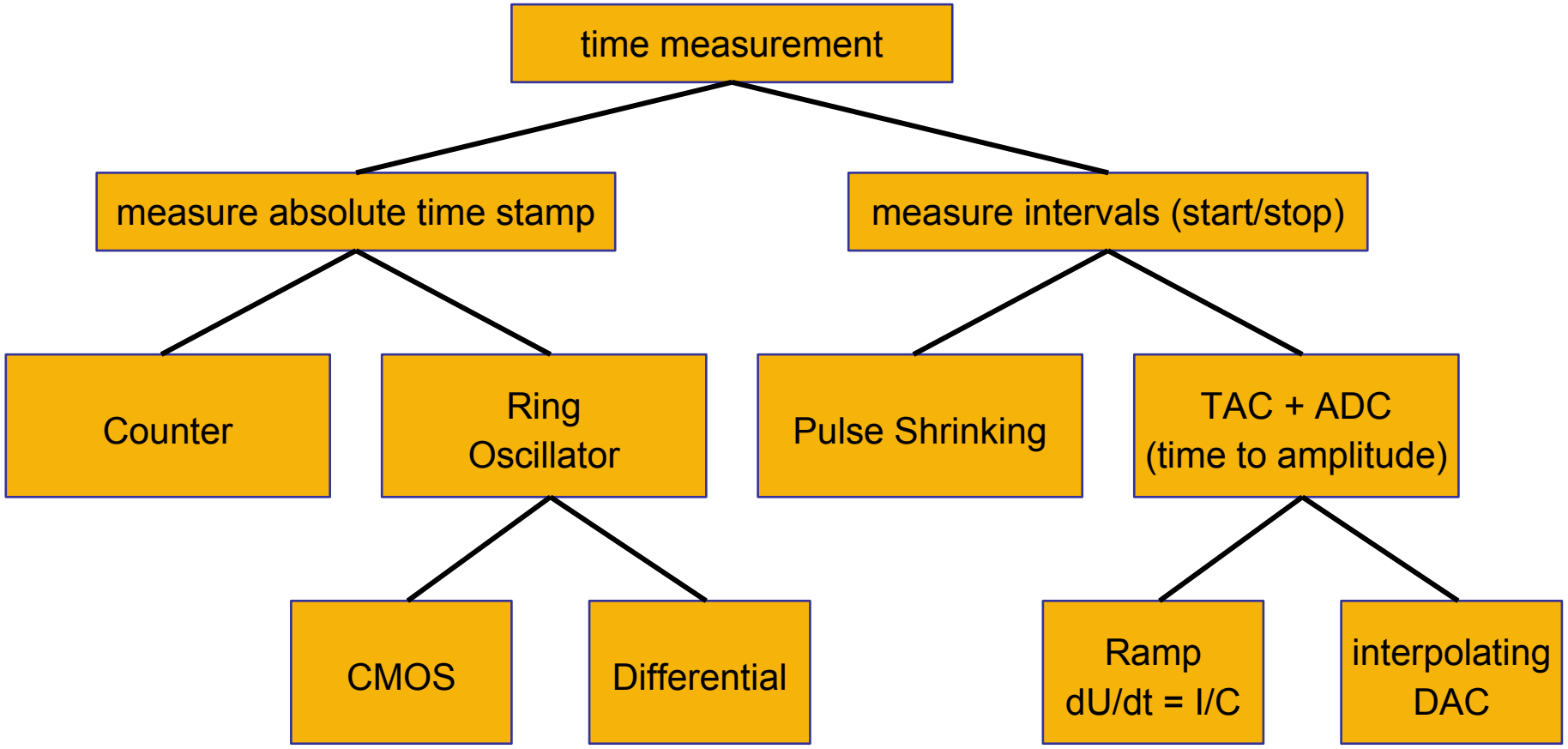
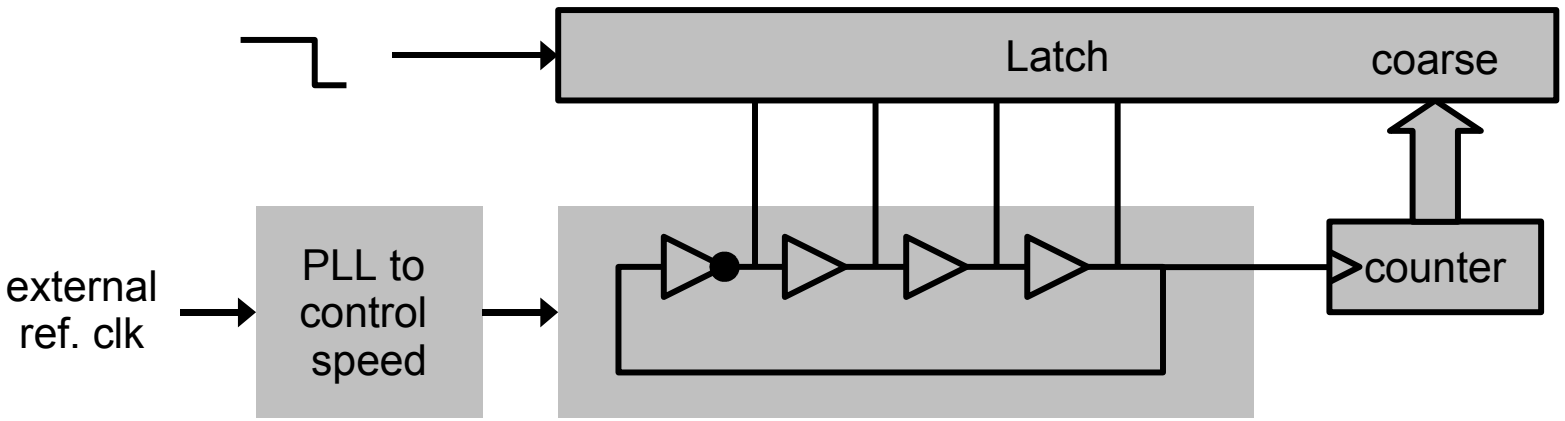
Overview of Circuit Concepts



... and mixtures of these concepts

Ring Oscillator: Principle



- Principle:
  - a ring oscillator generates thermometer code time stamps. Needs overall inversion!
  - a ("slow") coarse counter generates the MSBs
  - input signal is used to latch values
  - Ring oscillator can be locked to a reference clock with a PLL

\+ fairly simple, "digital" design

\+ infinite dynamic range

\+ no calibration required (with PLL), guaranteed stability

\- limited bin size (but several times better than with counter)

Ring Oscillator: Design variations

- Resolution can be increased by:
  - using multiple channels with delayed stop signals
  - running several phase coupled ring oscillators
  - using slow / fast buffers between ring oscillator and latches
- Use "single ended" CMOS logic
  - simple
  - issues: supply sensitivity, ring oscillator frequency range, linearity (inversion!)
- Use differential logic
  - uncommon
  - more complex, if everything is done differentially
  - trimming simpler

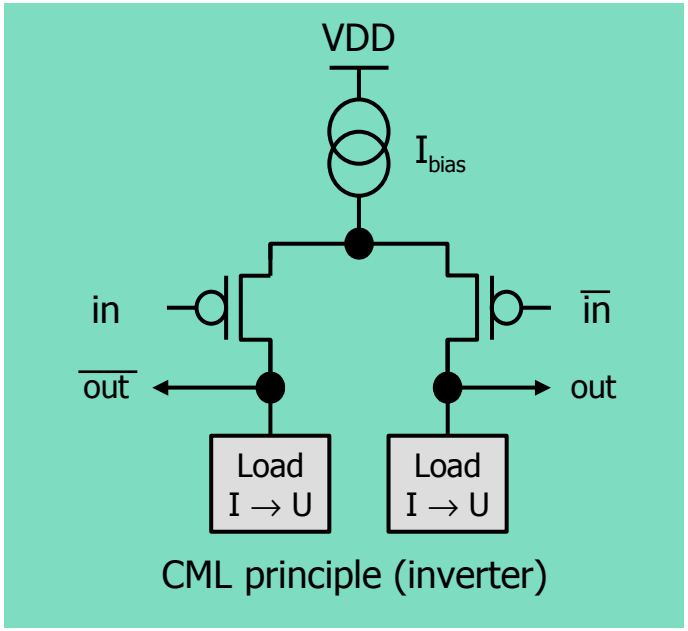
Design Issues

- Design goals are
  - minimal bin width = max. resolution (aim at σ = 20ps)
  - linearity
  - dynamic range
  - low dead time = high double hit rate (aim at 10 MHz)
  - low power (not so critical in Diamond: few channels, cooling possible, preamps and discriminators will be "high" power components)
  - easy calibration
  - stable operation (with temperature, power supply etc.)
  - multi-chip operation (maybe not required for diamond)

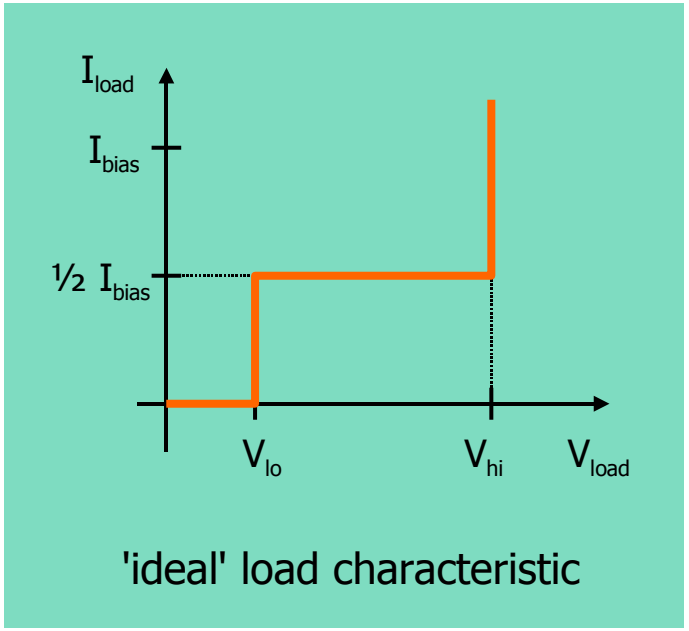
- Watch
  - matching between devices:
    better for larger devices, but that costs power and/or speed
  - radiation hardness
  - technology scaling (this favors "digital" designs)

Differential Logic

- Current I_{bias} is steered to left or right load circuit with a differential pair
- The load circuit converts to current step to a voltage step
- **'ideal' load** circuit:
  - The V_{hi}-level is fixed by the maximum possible input voltage to the switch block
  - The V_{lo}-level is fixed by the voltage swing required to 'fully' switch current in the switch block.
  - The plateau at $½I_{bias}$ guarantees equal rise and fall times (C_{load} is charged/discharged with $½I_{bias}$)
- If V_{hi} and V_{lo} are independent of I_{bias}, the speed of the gate can be varied significantly with I_{bias}



CML principle (inverter)



'ideal' load characteristic

Submission History

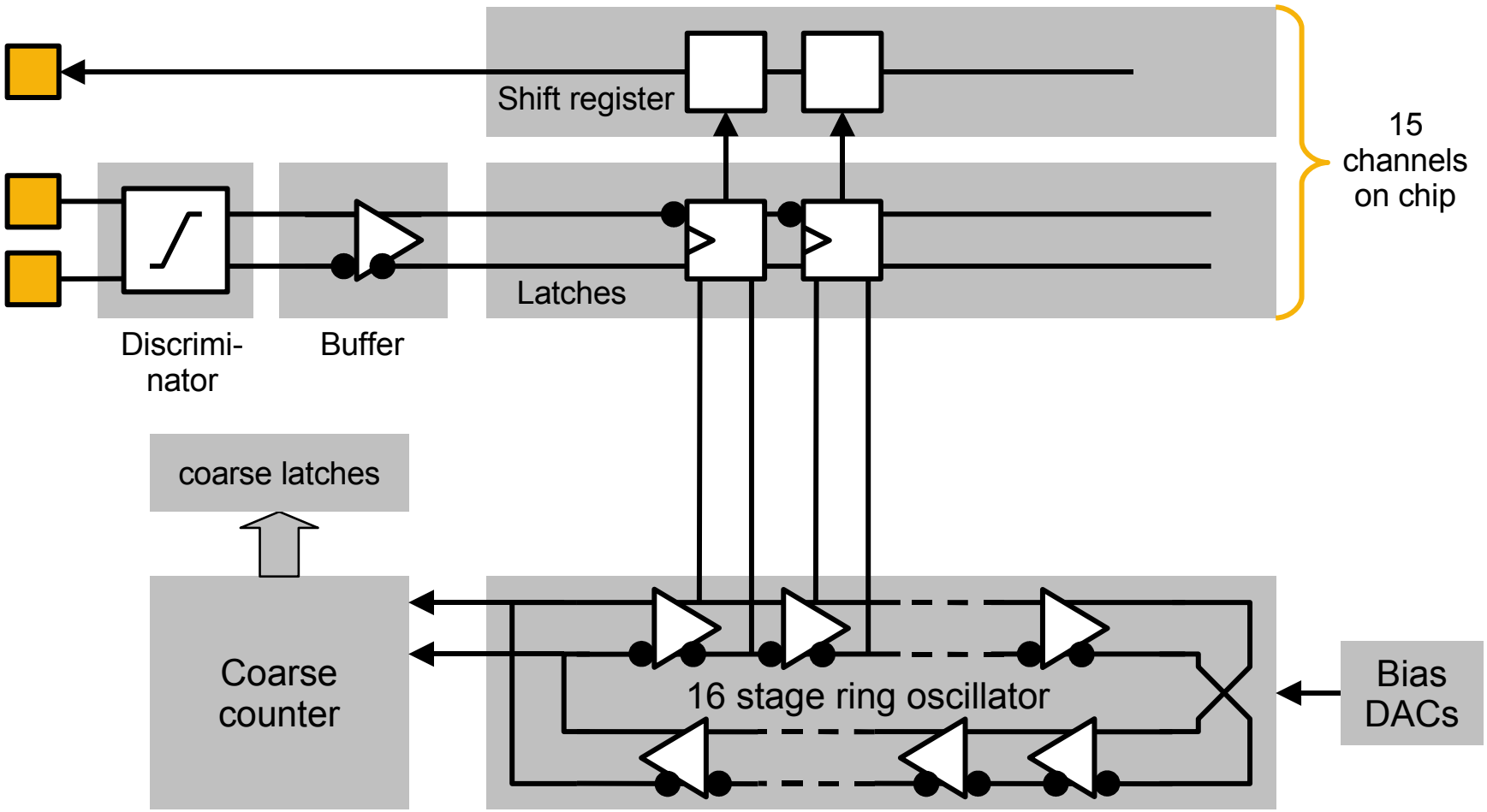
- **TC3**: AMS 350nm.
  Results presented here last year.
  Timing resolution $\sigma \approx 35$ps.

- **TC_UM1**: First UMC 180nm submission.
  Run paid for by GSI.
  Timing resolution $\sigma \approx 25$ps.

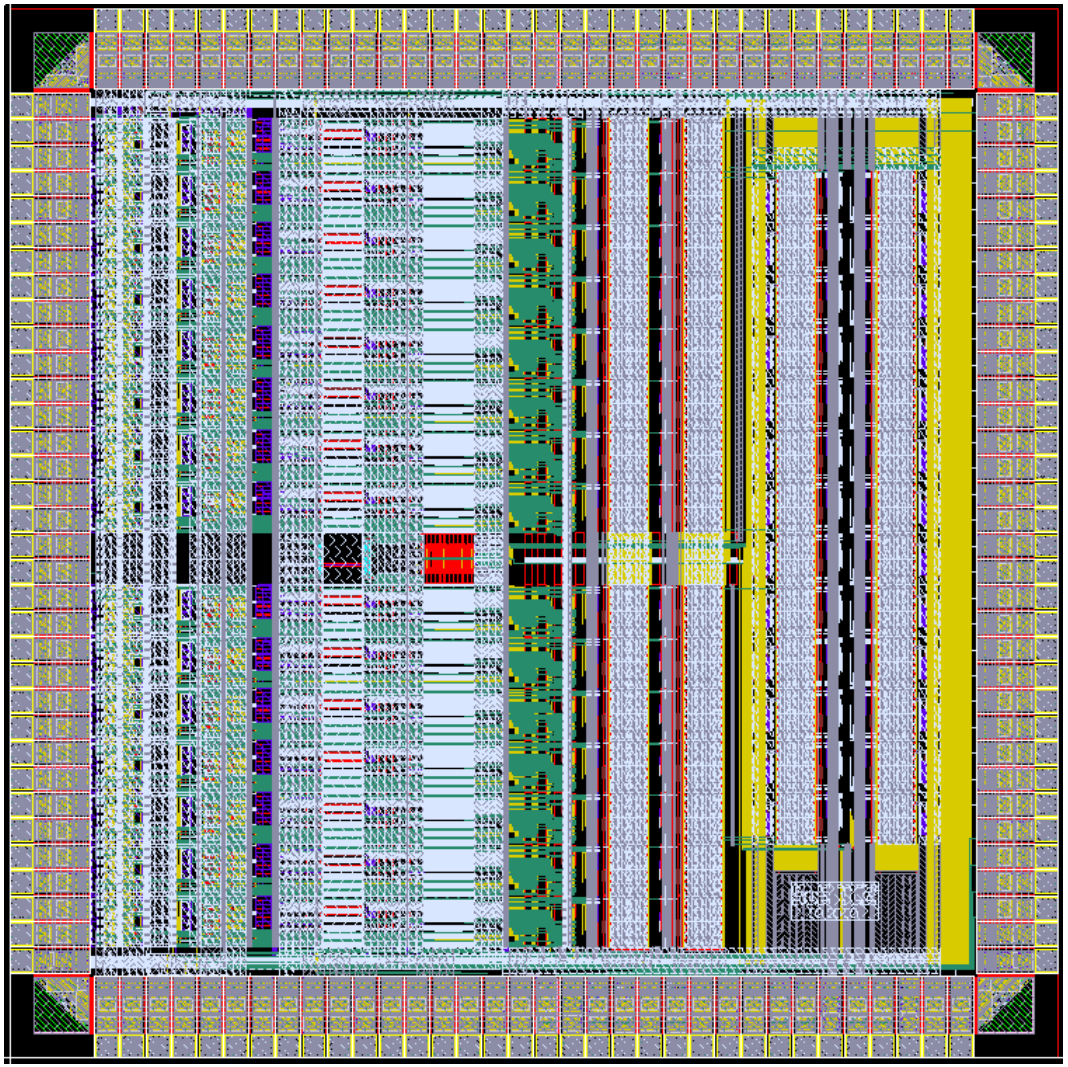
- **TC_UM2**: Current chip. UMC 180nm.

TC_UM2 Block Diagram

- Block diagram shows only relevant parts
- Note that the differential inputs have an additional (analog) discriminator on this chip



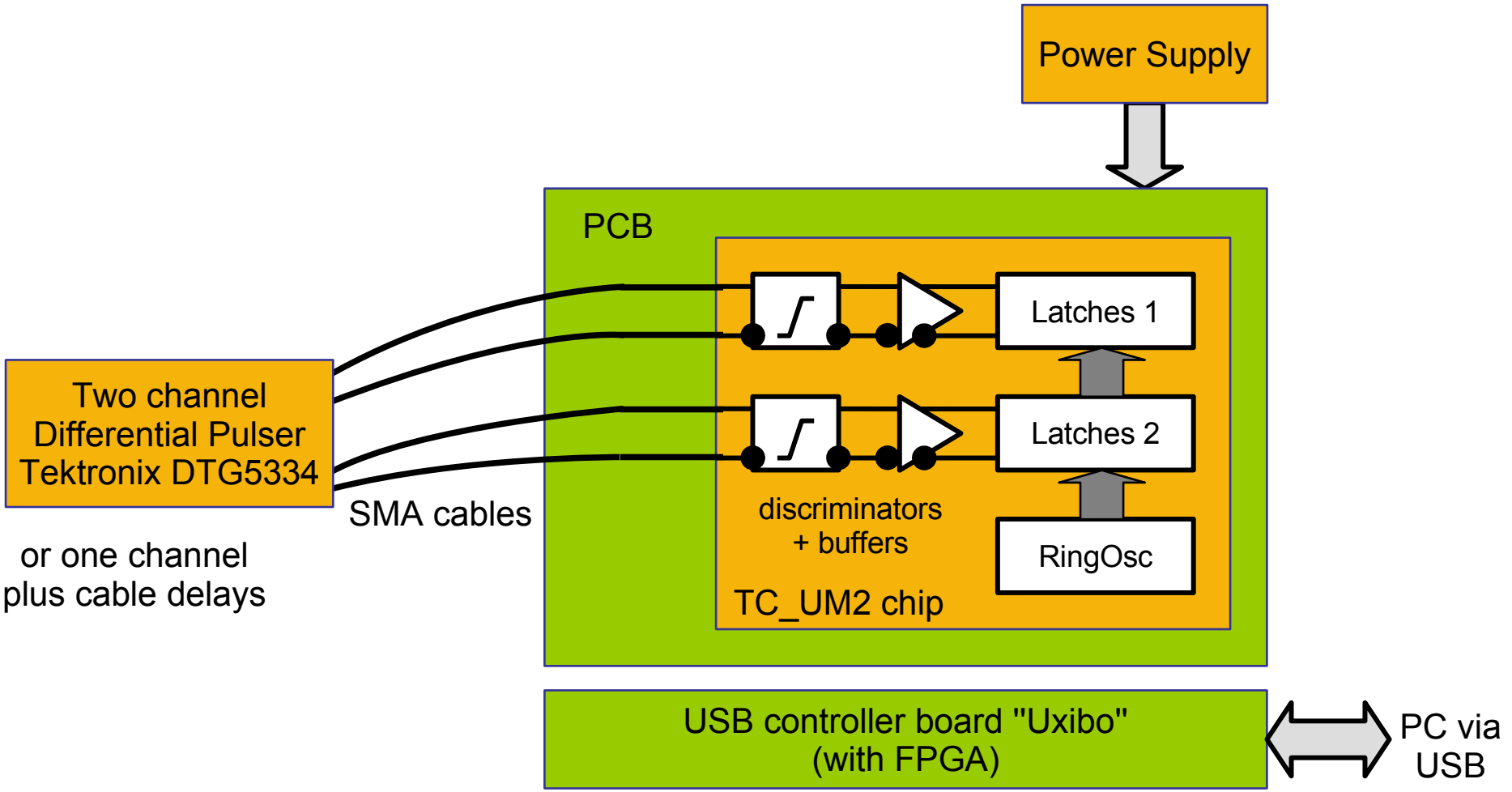
TC_UM2 Layout



- Size: 3.24x3.24mm^2
- 15 Channels

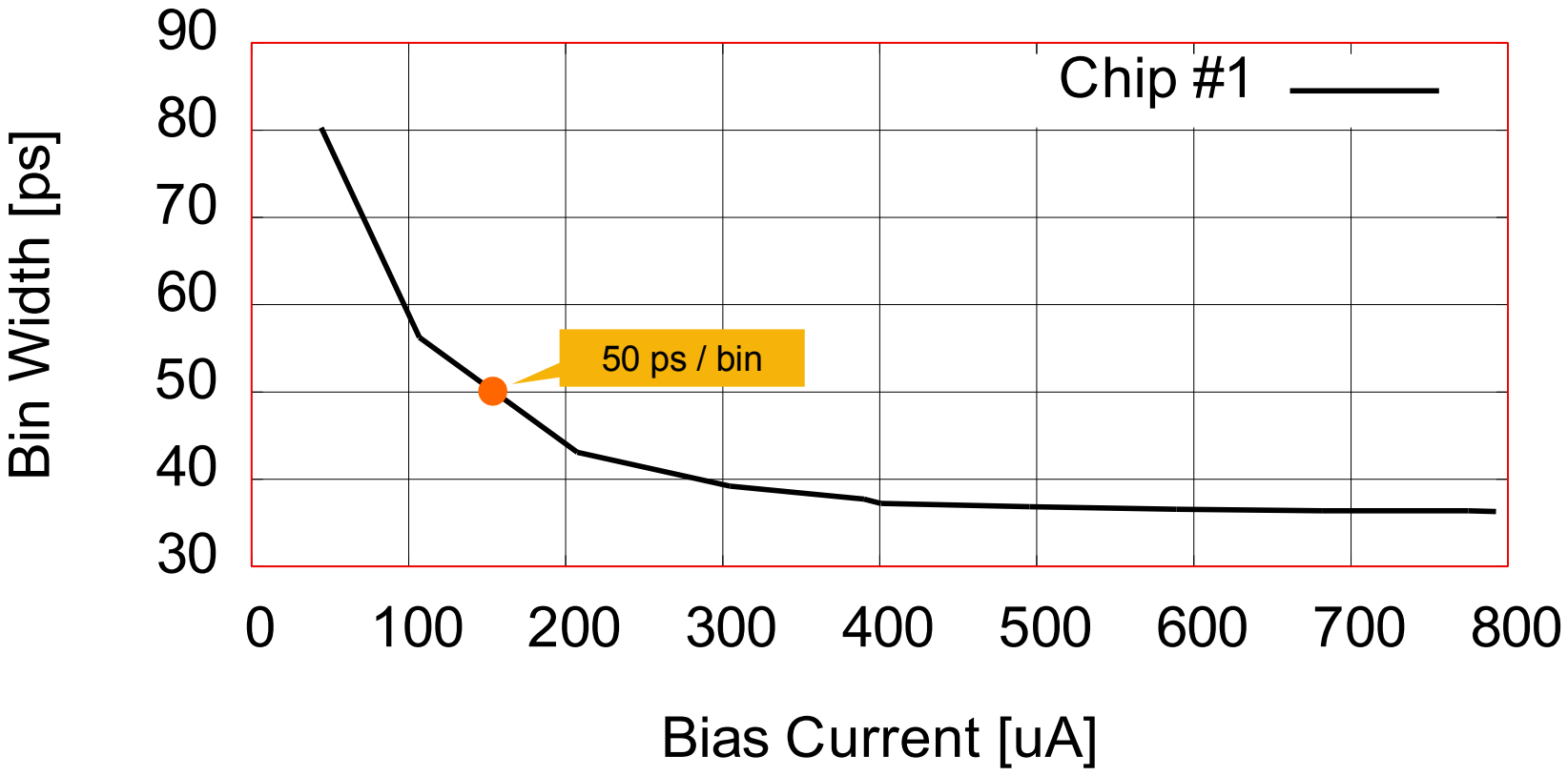
Test Setup

- We have developed a very compact USB based test setup.



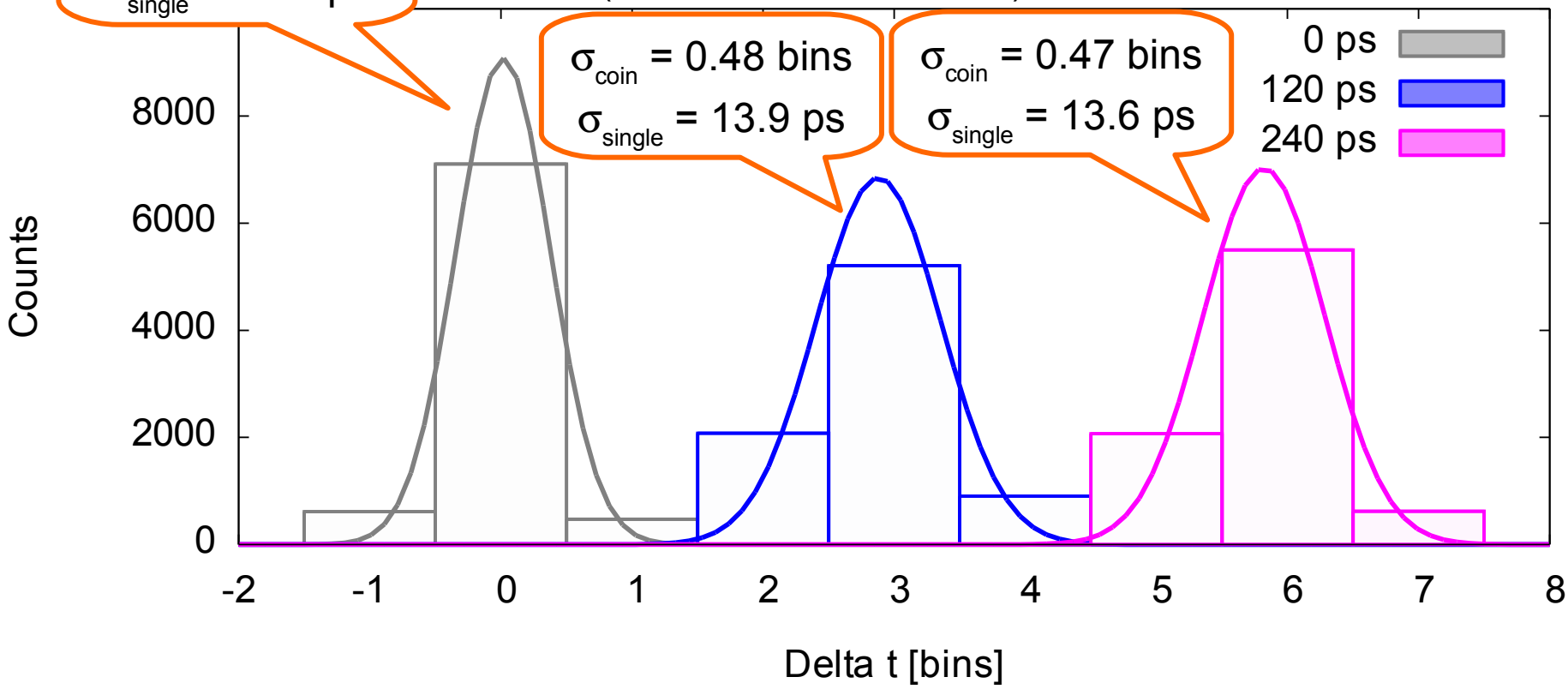
Measurements: Ring Oscillator Speed

- Accurate measurement of the VCO speed possible on a full-speed debug output
- Tuning range ~37 - 80 ps
- Standard operating point: **50 ps binwidth @ 160uA per stage** (from a 1.8V supply)



Hit bins for different delays

- Plot time **difference** (here in bins) for different delays
- Note that measured **coincidence sigma = √2 x single channel sigma**
- VCO speed was **~41ps / bin** for this measurement
- Plot shows results that have been **corrected for different bin sizes** (from transistor mismatch)



Summary

- We pursue a **ring oscillator** approach using **differential logic**
- Single channel resolution **σ < 20ps available today** in 180nm technology
  All non-linearities are included in this figure!

- Advantages of the ring oscillator are:
  - stability (if locked to reference frequency with a PLL)
  - "infinite" dynamic range (with wide "coarse" counter)
  - very small dead time
  - fair power consumption (<20mA @ 1.8V per channel + VCO)