Fast Signal Processing: From the Detector to the TDC, an experimentalists (non expert) point of view

Wolfgang Koenig for the HADES Collaboration

Menu:

- **Diamond Detectors at Hades (Boundary conditions)**
- **Signal / Noise & Risetime: general considerations**
- **Response of fast MMICS Amp's (Measurements and Simulation)**
- **A Proposal for optimized MIPS Diamond detectors (Simulation)**
- **Discriminator measuring Signal Time and Charge simultaneously**
- **New HADES TDC board**
- **A Proposal for a 10 Ghz (peak Intensity) HI Diamond Detector Set**
- **Summary, Acknowledgment**

Chairman will stop me

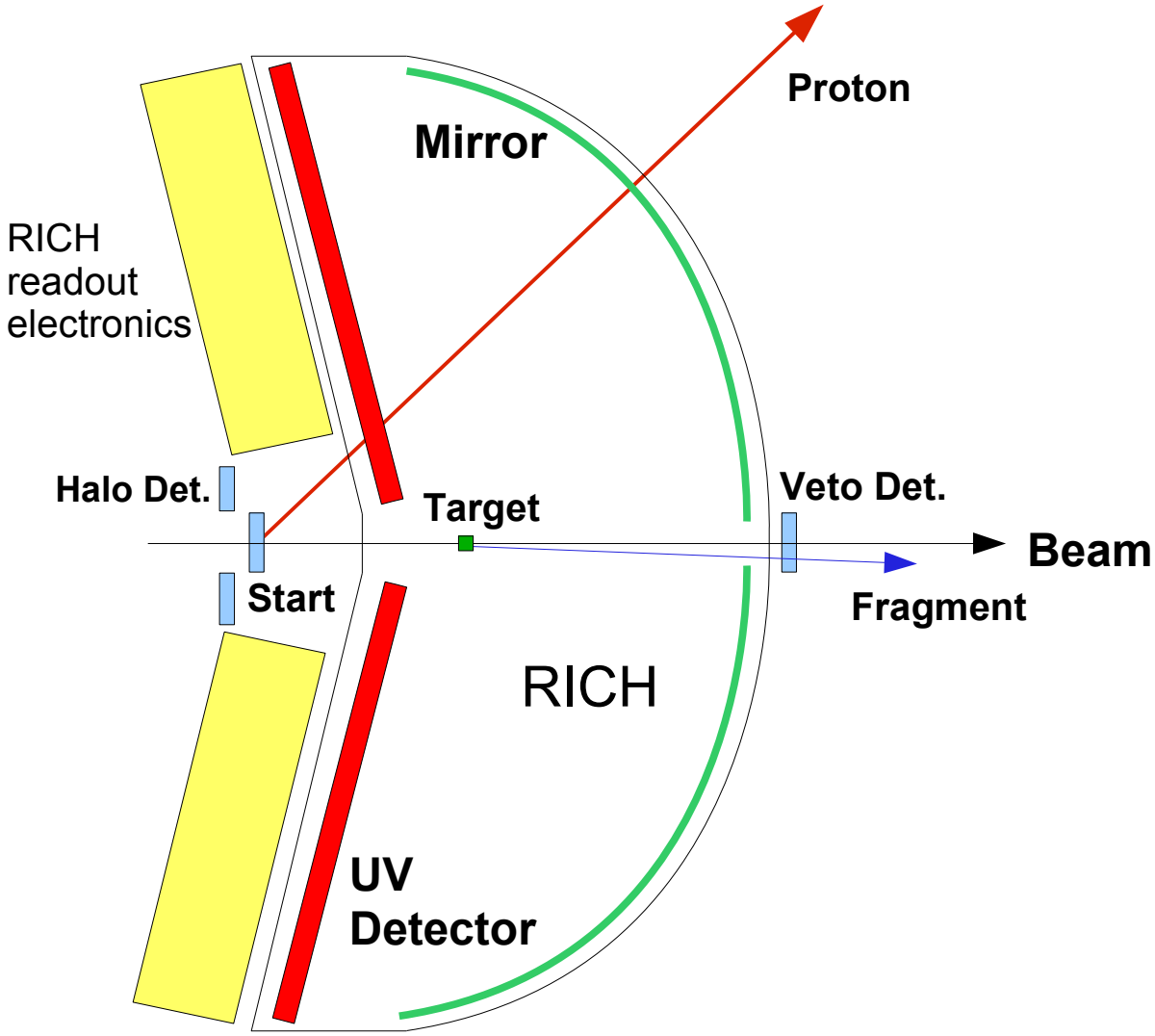
Diamond Detectors at HADES:
Requirements and Boundary conditions

Requirements

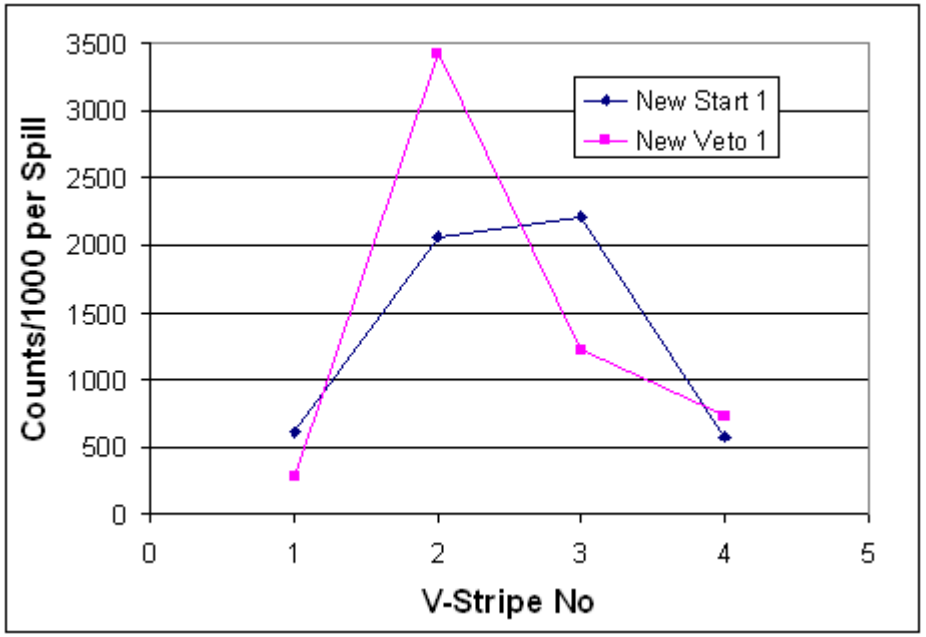
- Beam diagnostics
- Beam Intensity Monitoring
- Time reference Signal
- Reject peripheral collisions

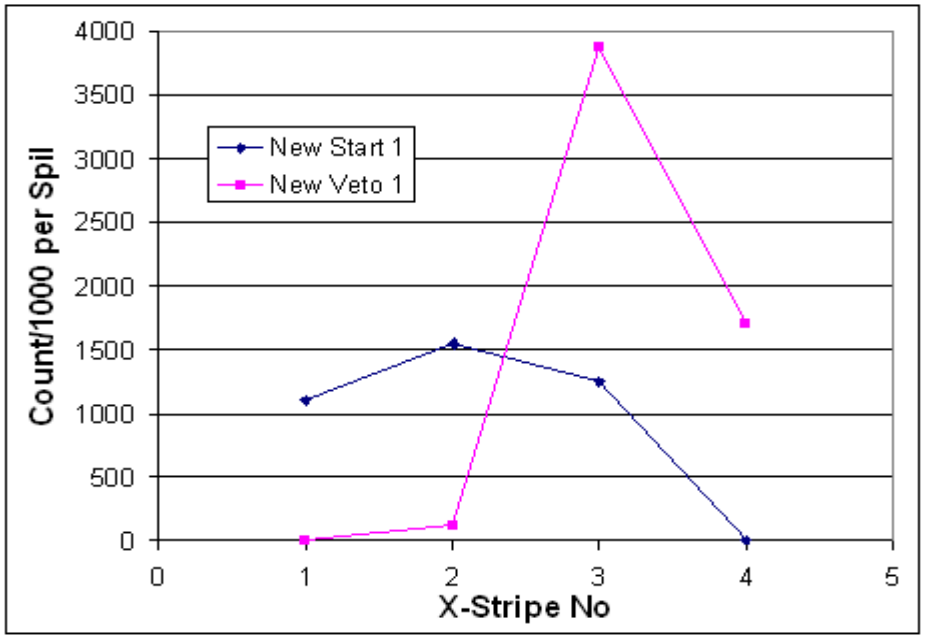
Boundary Conditions

- Minimize RICH Load
- Do not spoil 2nd Level Trigger
- Ignore Noise from other Detector Systems



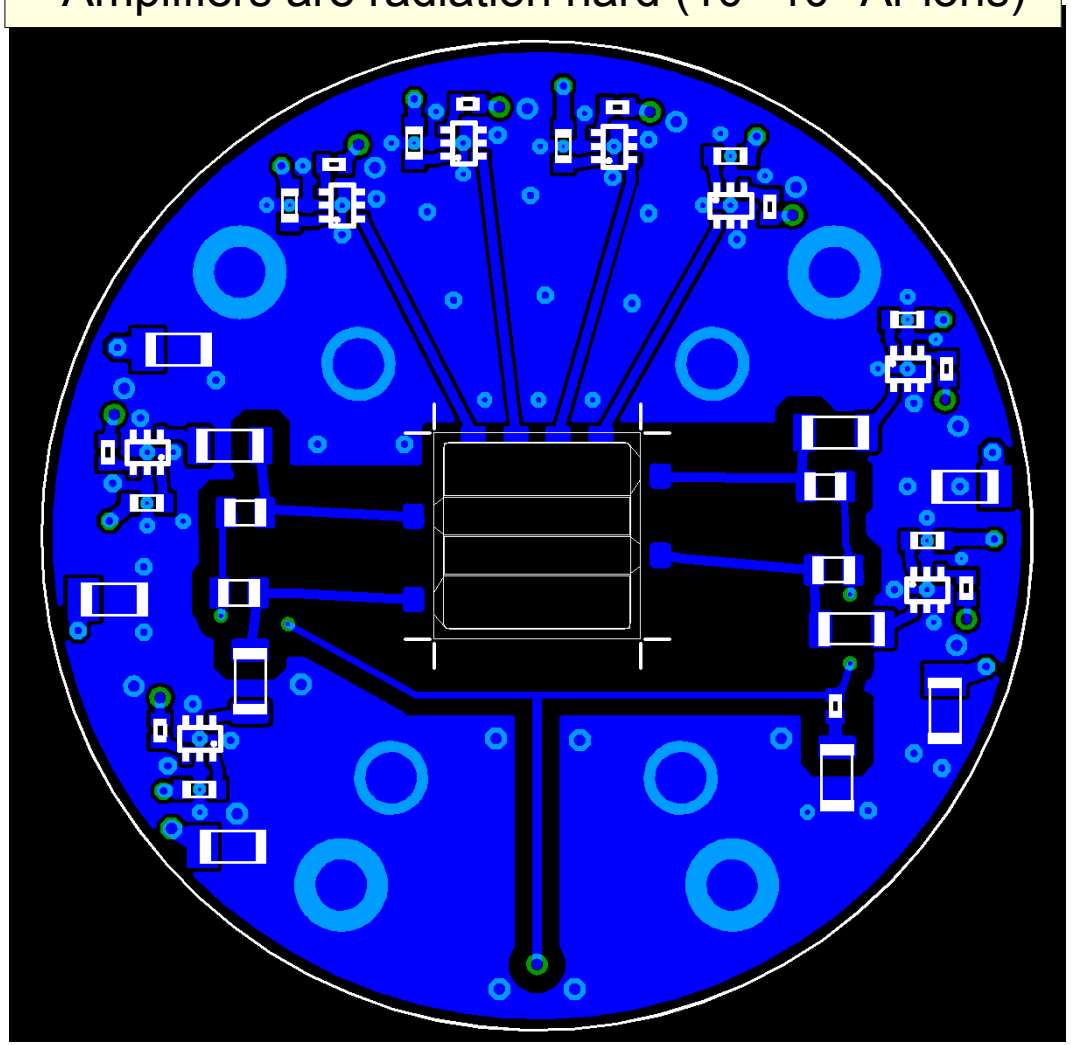
50 µm Diamond, 4 X-Stripes (front), 4 y-Stripes (back), integrated preamps





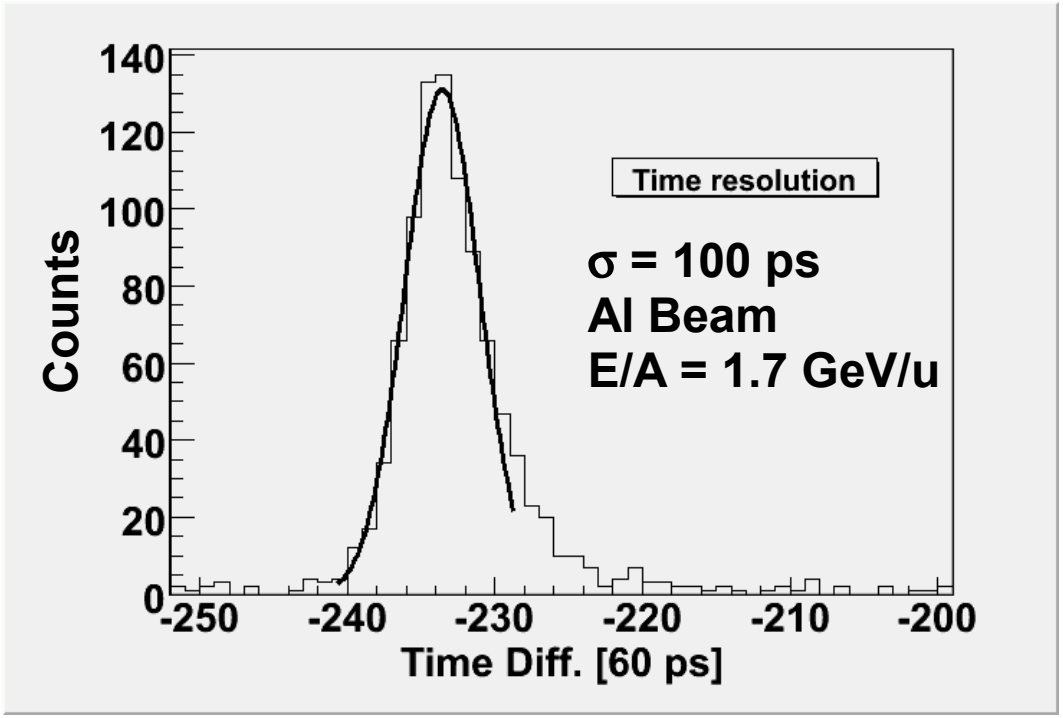
Vertical and horizontal beam profiles (AL-Beam)

- Efficiency Start: > 98%
- Veto removes 95% of Start signals (3% interaction length target)
- Amplifiers are radiation hard (10^6-10^7 Ar ions)

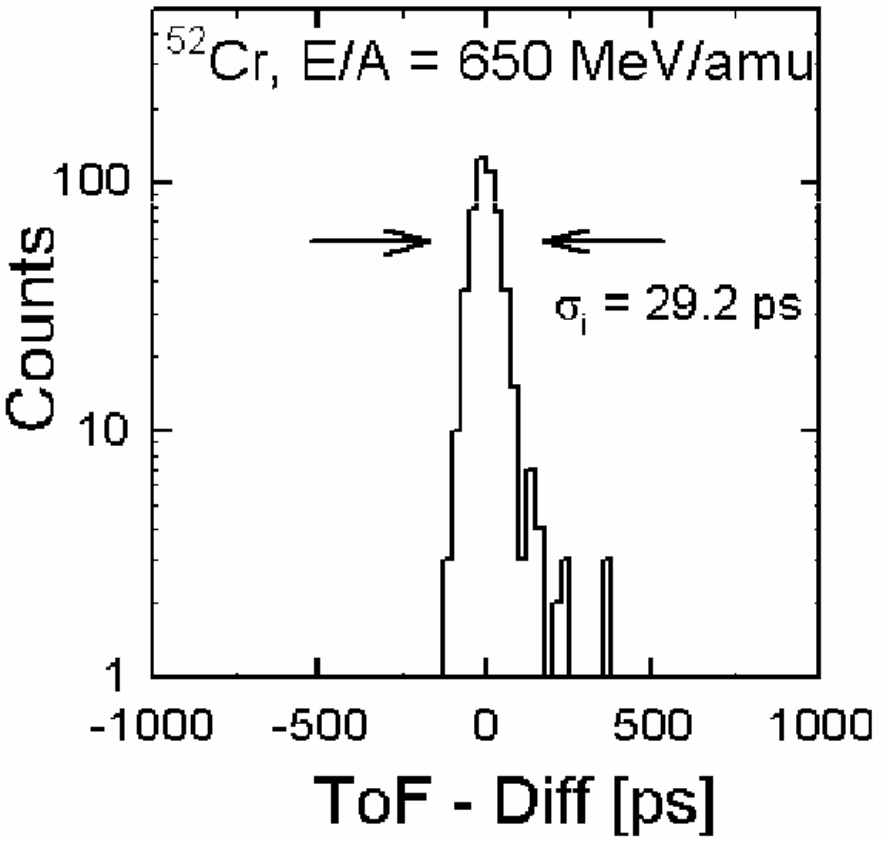


PC-Board: 0.2 mm thick, 48 mm Diameter
Diamonds provided by R. Gernhäuser

Time resolution



50µ detector, readout on both sides (2*4 stripes)
Large beam induced leakage currents (>factor 10)
with decay constant of several minutes
10 years old booster stage



100µ Detector, single sided readout
(8 stripes)

- **Unexpected bad time resolution**
- **Signal ca. Factor 4 below expectation**

Basics

Ideal (noise free) amplifier with input impedance R:

Noise: $\sqrt{4kTR\nu}$

k= Boltzmann Constant, T= Temperature, R= Resistor Value, ν = frequency

Noise Figure:

Real amplifier provides further Noise (specified in DB, logarithmic scale)

Some Noise figures for MMICS (Monolytic Microwave Integrated Circuits)

MMIC Type	Noise Figure	Voltage Noise increase
BGA2712	3.9	**1.57**
BGA2748	1.8	**1.23**
GALI - S66	2.9	**1.4**
BFG310	1.0	**1.12**

Noise close to ideal amplifier

← Transistor

MMIC Type	Measured Rise Time [ps]	Frequency Range [Ghz]	Calculated Noise [µV]	Measured Noise [µV]
BGA2712	140	1 -3	**20.7**	**24**
GALI - S66	350	0.4 – 1.2	**13.1**	**13**

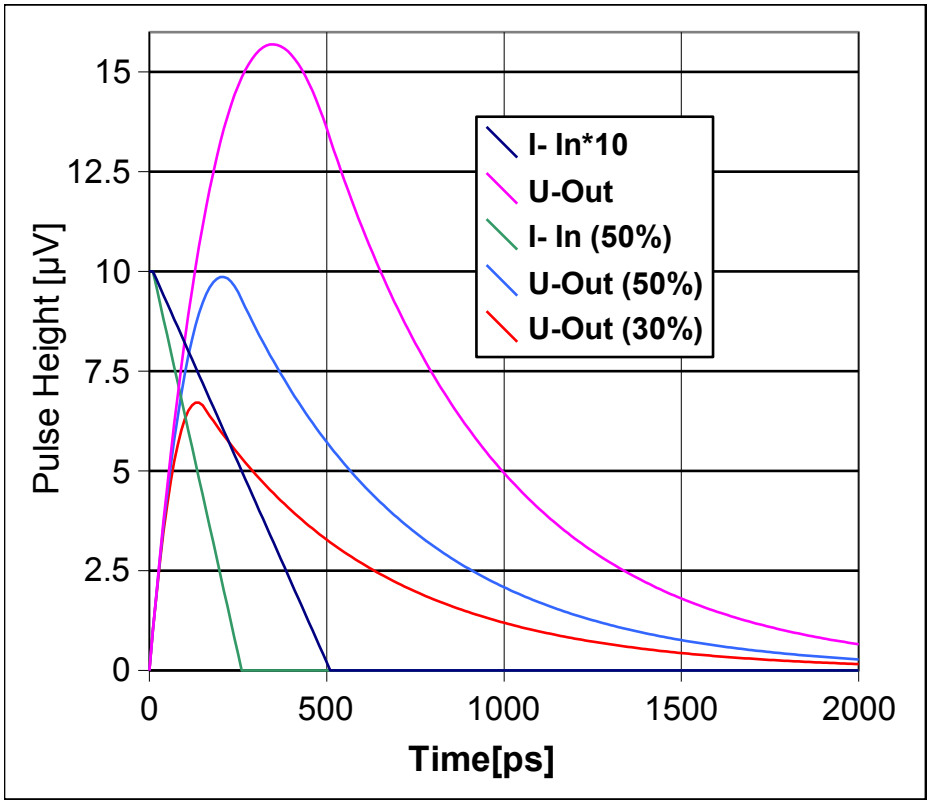
Measurements done by Andrei Caragheorgheopol

Detector Response (Toy Model)

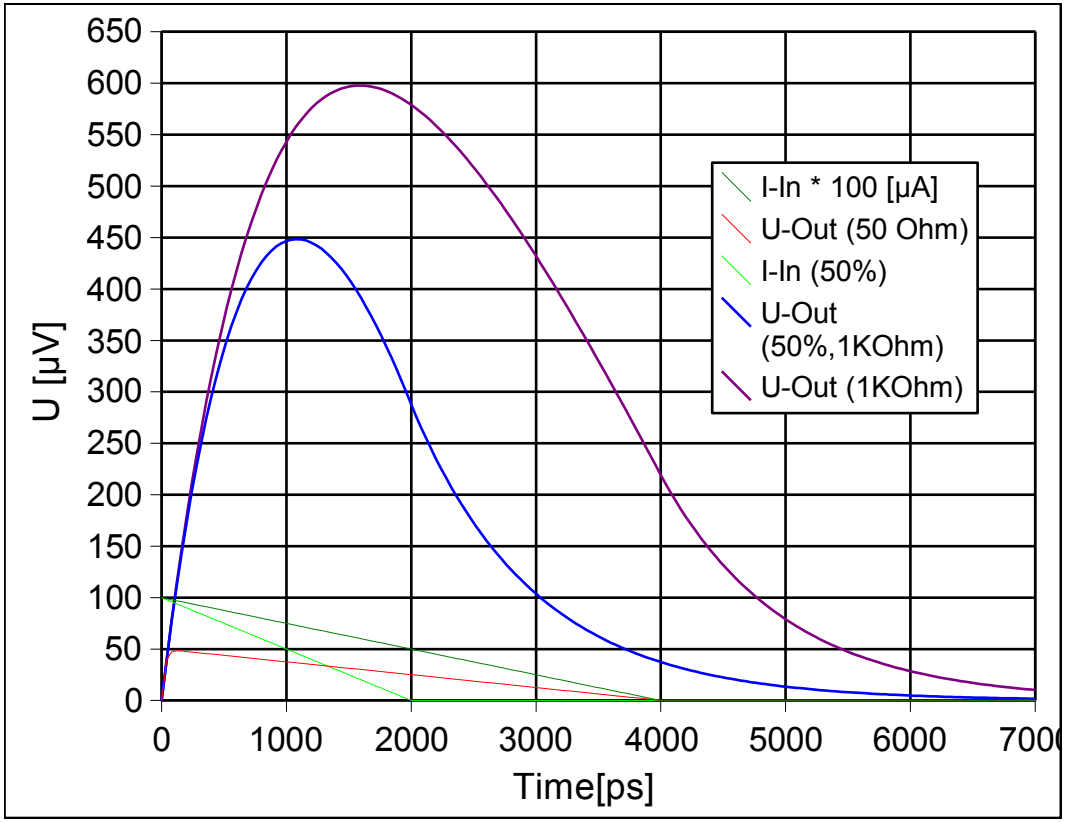
Induced current:

$I(t) = 2*Q_{tot}* v_{Drift} / d * (1 - t/T_{max})$ I_{MAX} = 1.2 µA for MIPS (used 1 µA), **v_{Drift}** = 1ns/100µm

Q_{tot} = total electron charge created, d = detector thickness, T_{max} = maximum drift time



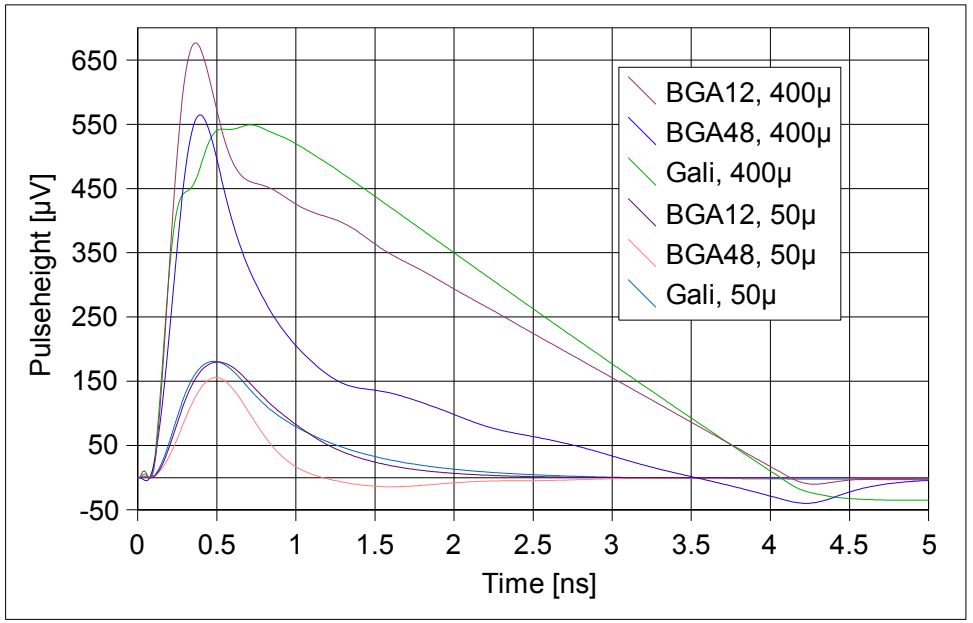
50 µ thickness, 10 pF capacitance
(10*10 mm² , 4 stripes)

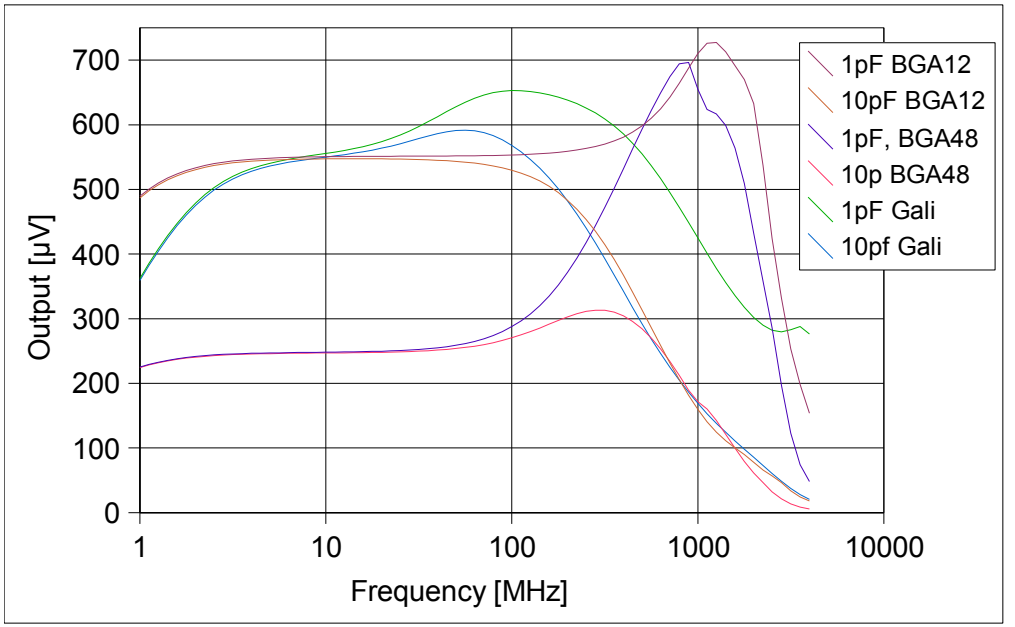


400 µ thickness, 1 pF capacitance (different Y-scale)
(3*3 mm²)

Comparison of a 50µ and a 400µ Diamond (fast and medium fast amplifiers with 50 Ohm impedance)

Input: 1µA Peak Current, 4ns linear decay time (400 µ), 0.5ns (50µ)





MMIC	Signal [µV]	Noise [µV]	Measured Noise [µV]	Ratio S/N	Risetime [ps]
BGA12, 400µ	677	396		**1.71**	**165**
BGA48, 400µ	565	263	192	**2.15**	**192**
Gali66, 400µ	549	271	184	**2.02**	**292**
BGA12, 50µ	180	174		**1.03**	**237**
BGA48, 50µ	156	106		**1.48**	**243**
Gali66, 50µ	181	157		**1.15**	**230**

Measured noise not corrected for limited frequency range and 2 stage amplification

Simple Signal / Noise Considerations:

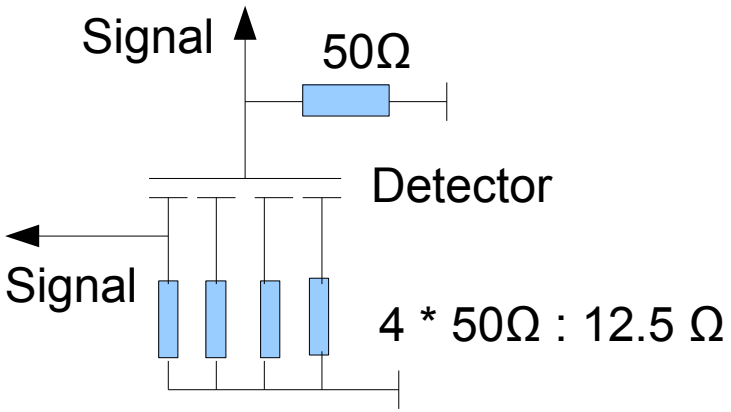
- 1 µA peak current in 50Ω (1pF): 48 µV
- measured input noise (fast MMIC): 24 µV

Signal / RMS-Noise = 2

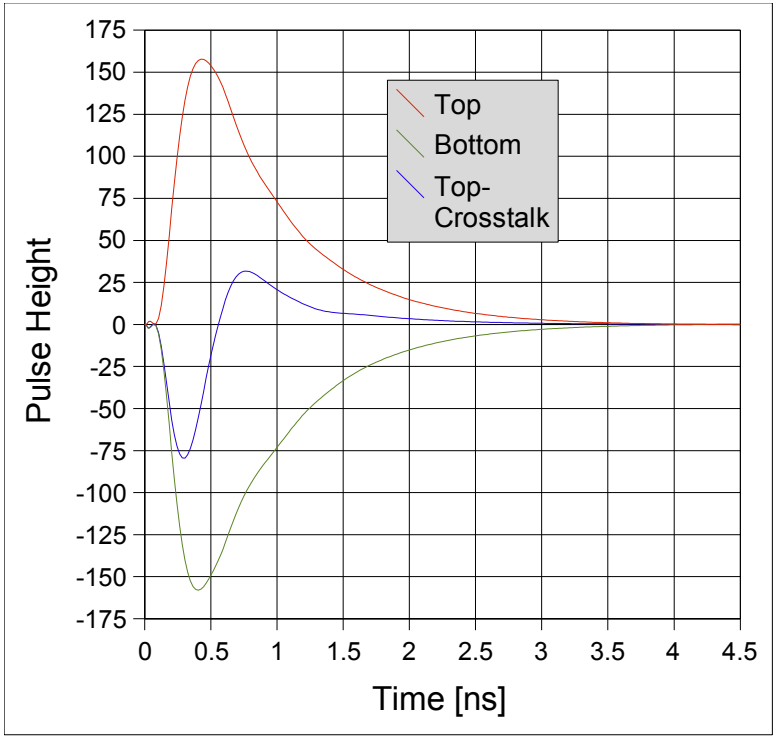
Trigger Threshold >= 5 * RMS Noise

➡ Signal / Threshold = 0.4 @ 1µA Peak

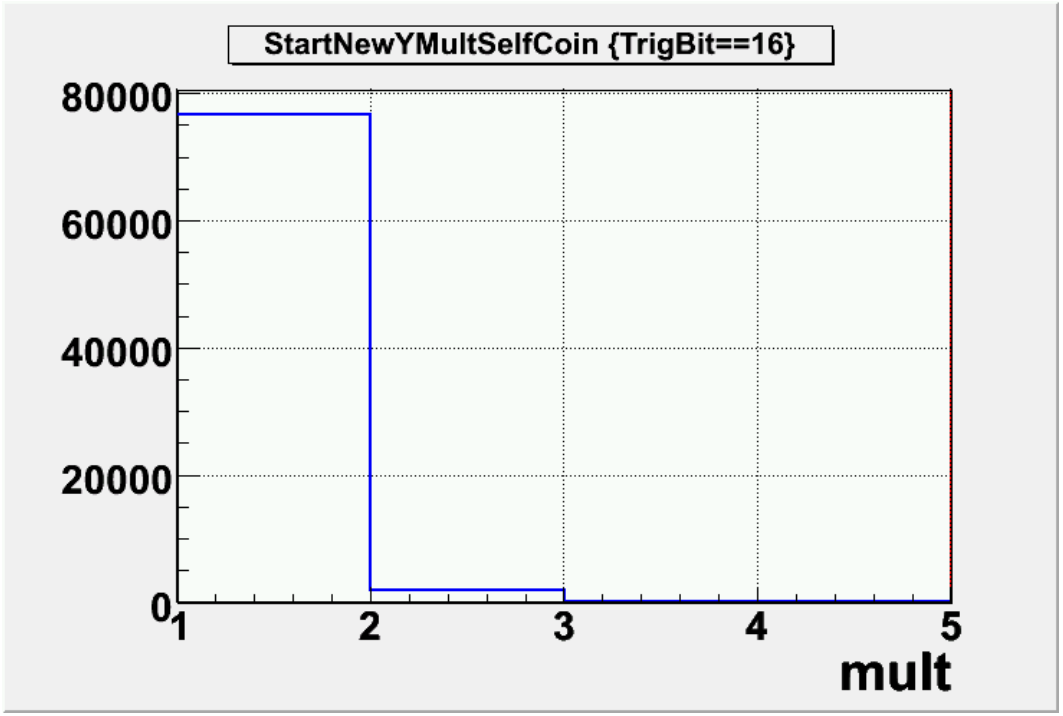
Readout from both Sides (Crosstalk)



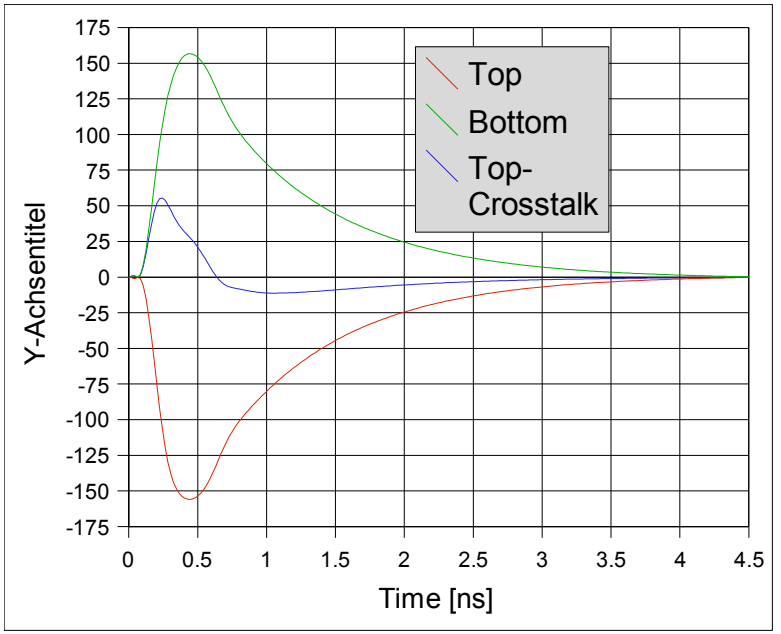
- 25% attenuation due to two sided readout (4 Stripes)
- Inverted (bipolar) signal on neighbored stripes



BGA2712 (fast response on bipolar crosstalk)

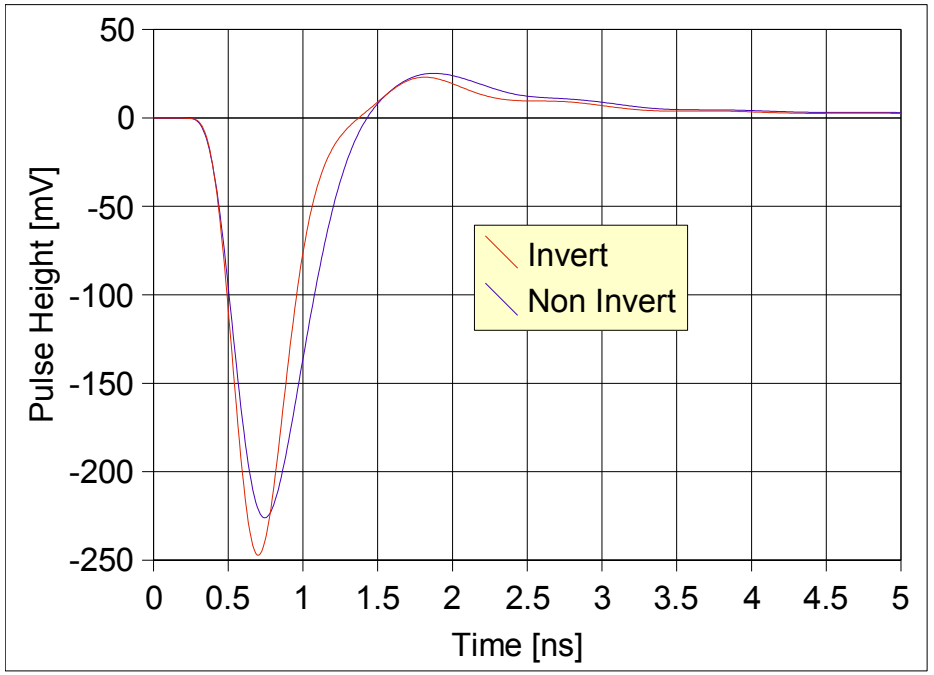


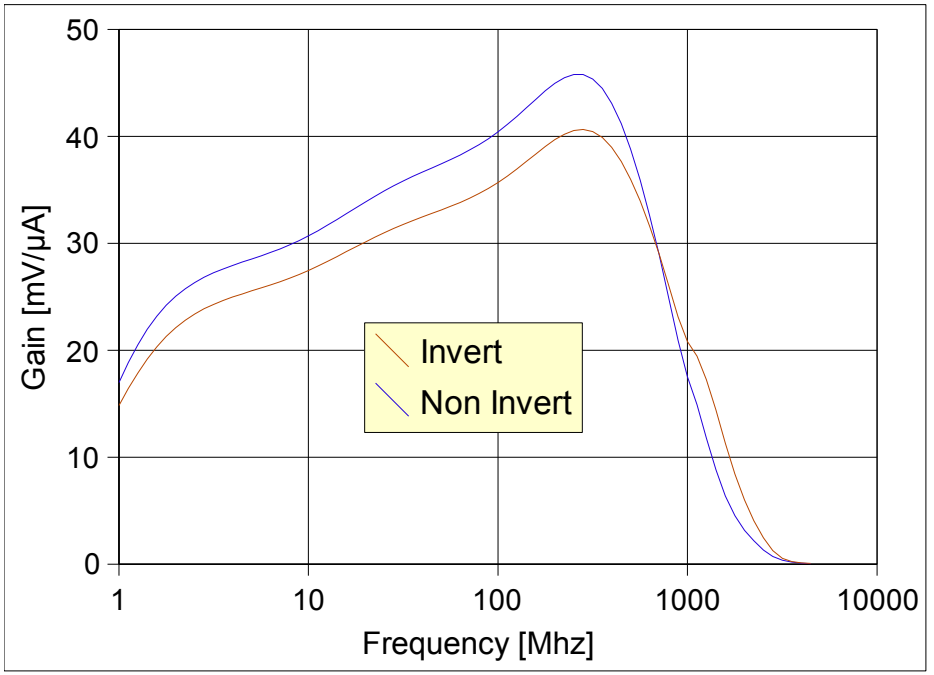
Measured crosstalk
(Stripe Multiplicity, Ar Beam, 10^6/s)



Gali-S66 (inverting, crosstalk reduced by factor 3)

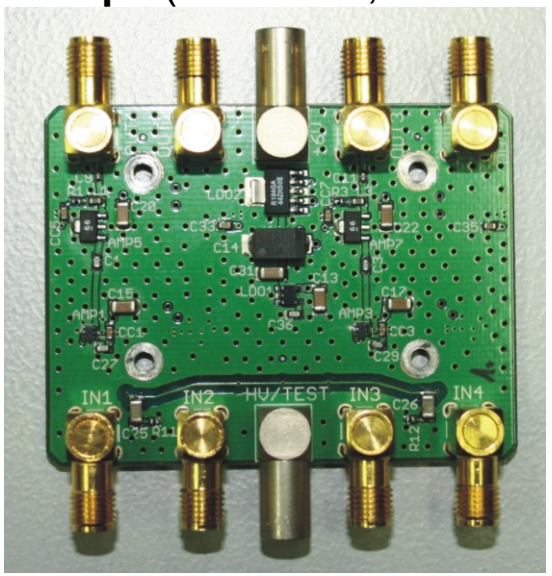
3 Stage Amplification (Inverting and non Inverting)





Rise Time: (Input Pulse: 0.25 ns decay time, 20µA peak, 10pF)

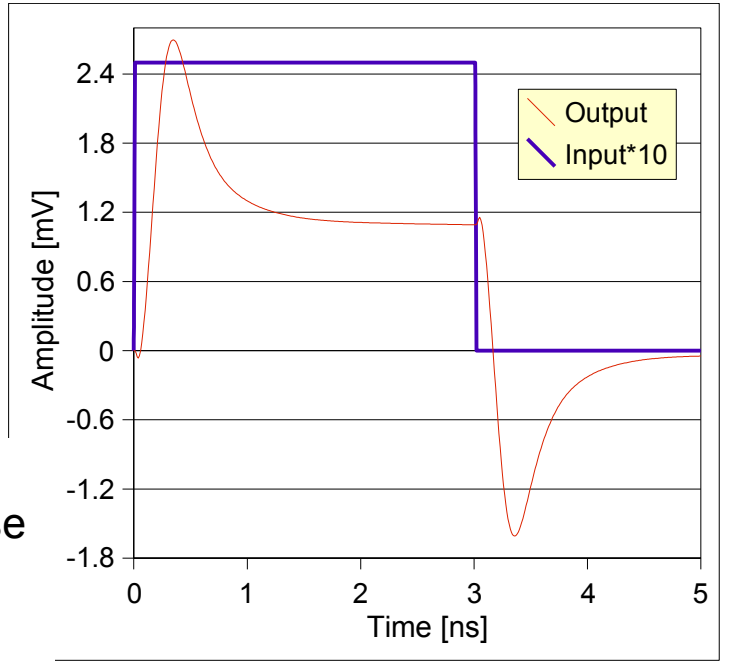
- **230ps** (Invert, BGA2748, BGA2712, Gali-S66)
- **260ps** (non Invert, BGA2748, Gali-S66, Gali-S66)



4 fold Amplifier
BGA2712/Gali-S66
with HV / Test input
Supply: 5.5 to 12V

Rectangular Test Signals:

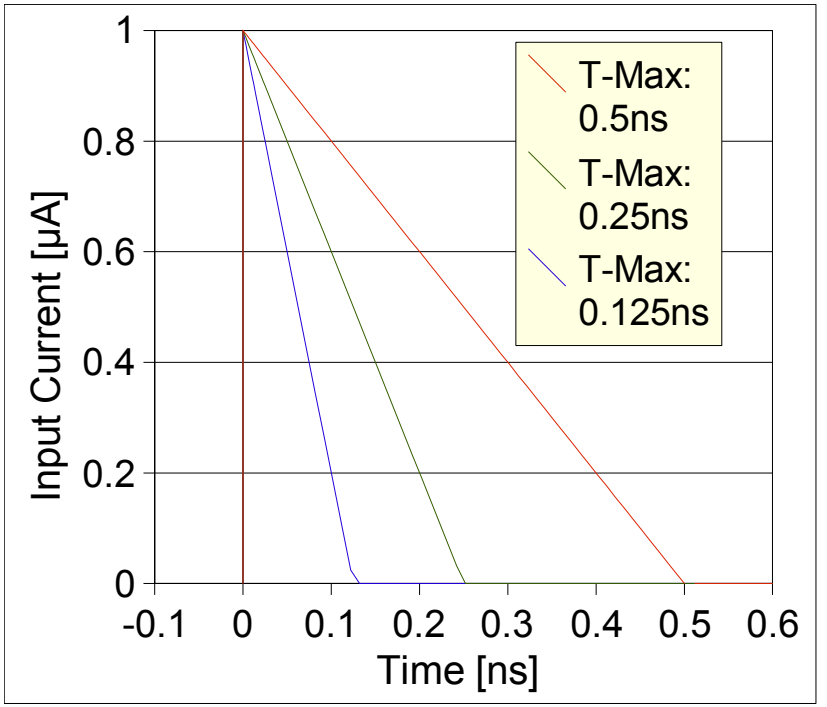
- BGA2748: misleading response
- Gali-S66: 360 ps rise time agrees with measurements



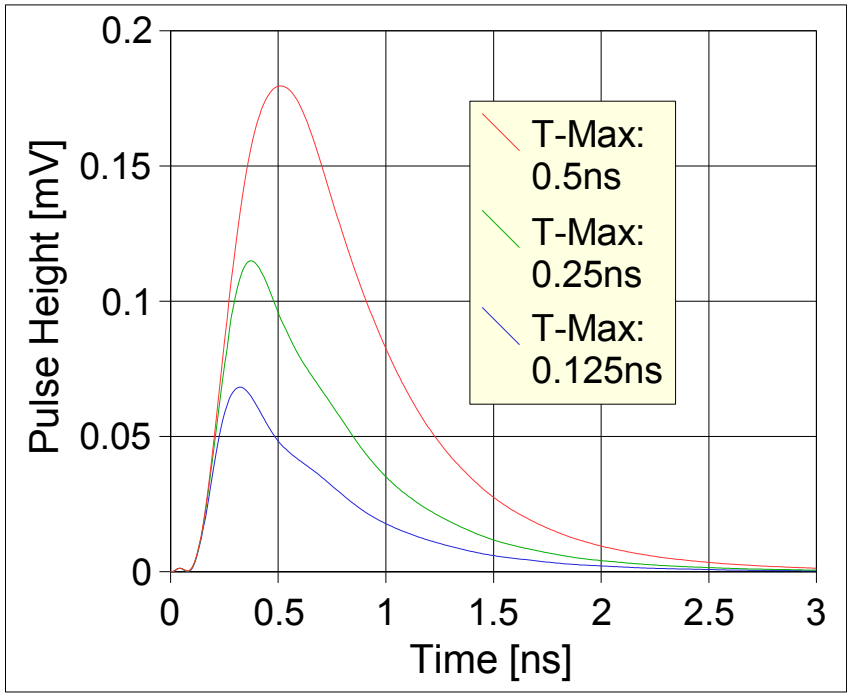
Effect of charge losses
(polycrystalline, 50 µ Detector)

- Leading edge discriminator best suited
- Rise time decreases with increasing losses (τ_R (poly) < τ_R (single crystal)

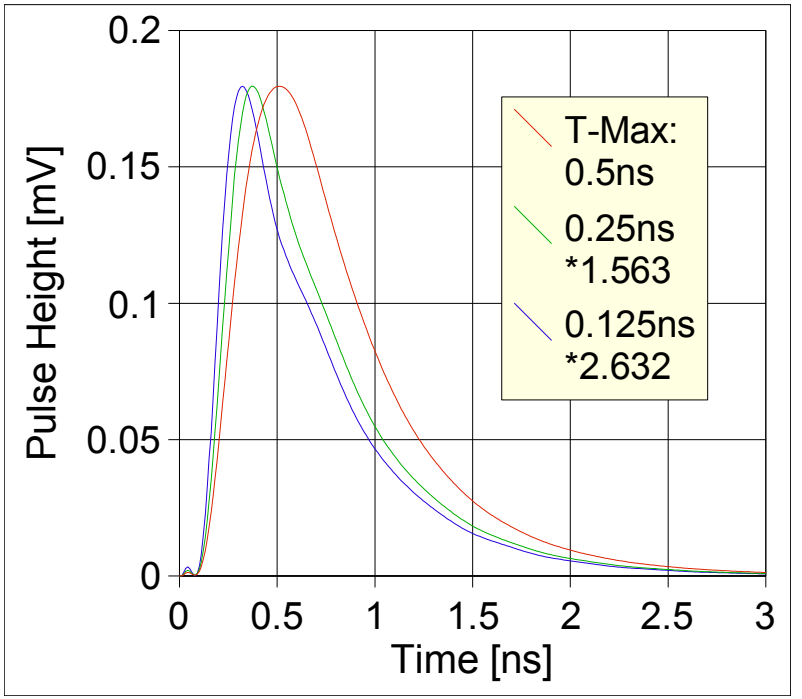
Induced current



Output signal distribution (BGA2712)

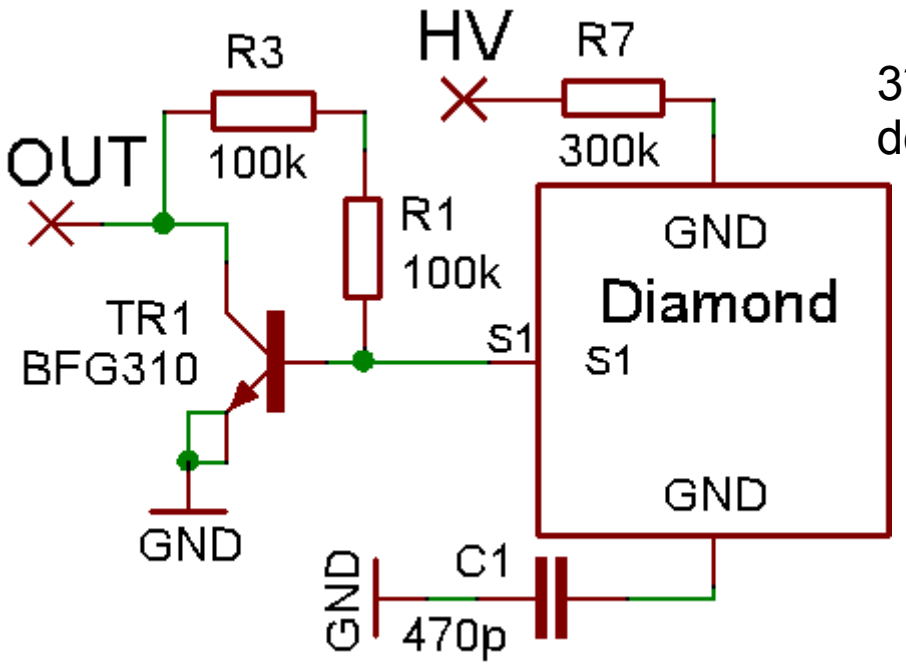


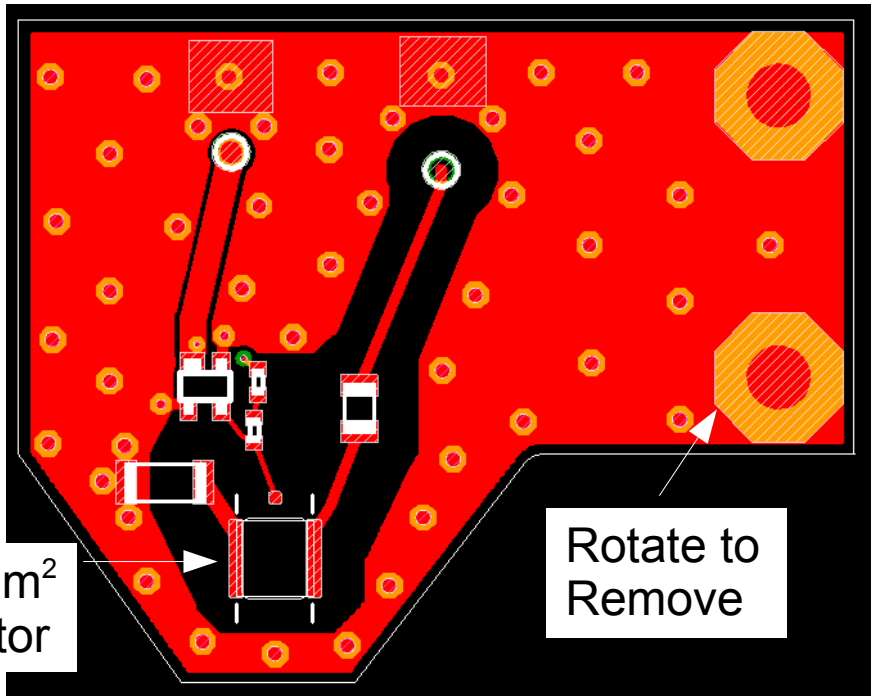
Normalized output signals

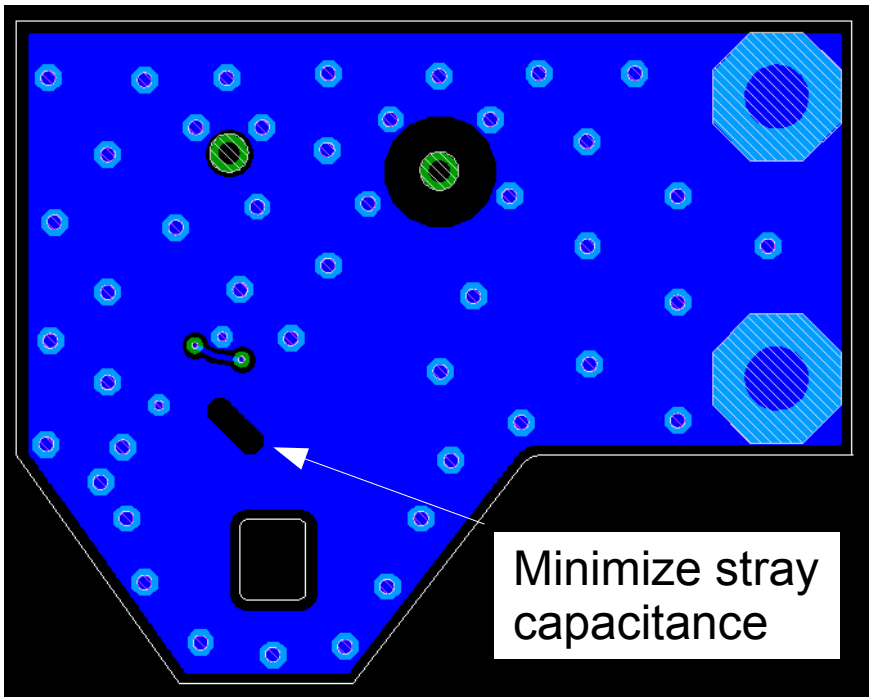


Layout of a Diamond Detector with a Transistor Amplifier (ca 1kOhm impedance) attached.

RF transistor (Feb. 2005, 14GHz)
- low noise (Noise Figure = 1)
- low input capacitance (0.16pF)



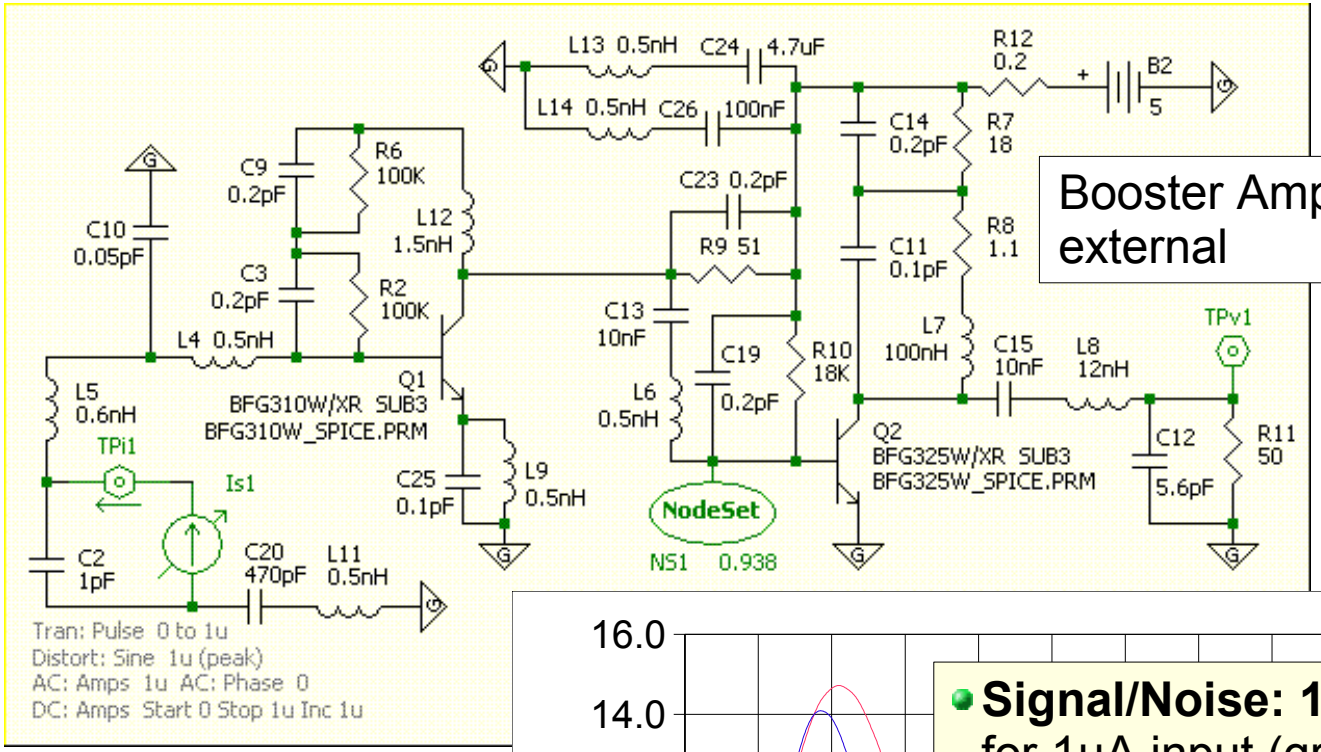




- Low Power Consumption: 10 mW / channel (5 V, 2 mA).
- Bias Voltage supplied via Signal cable

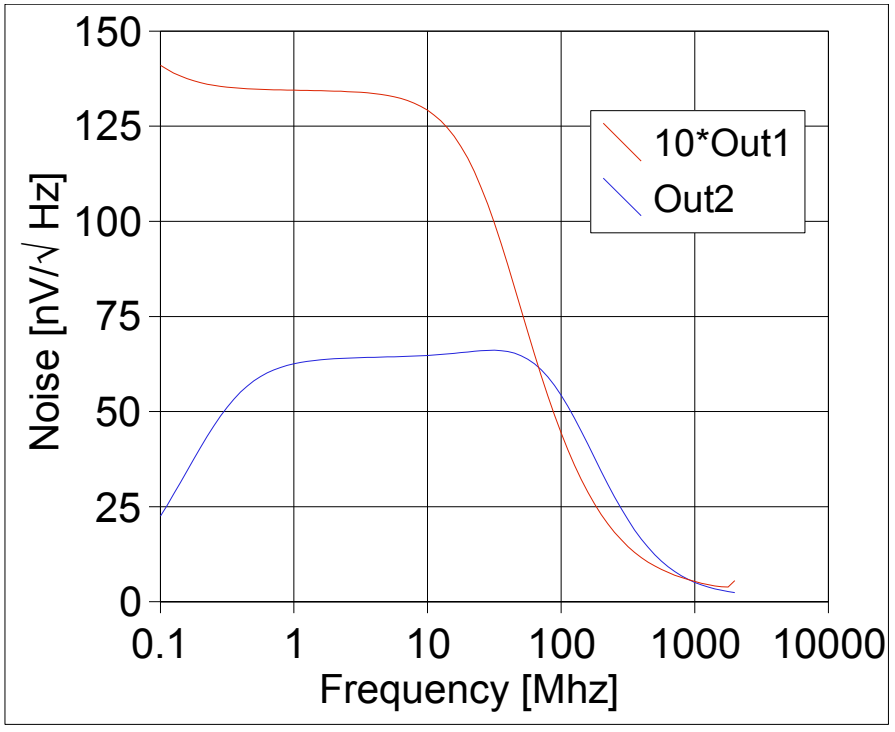
Spice Simulation

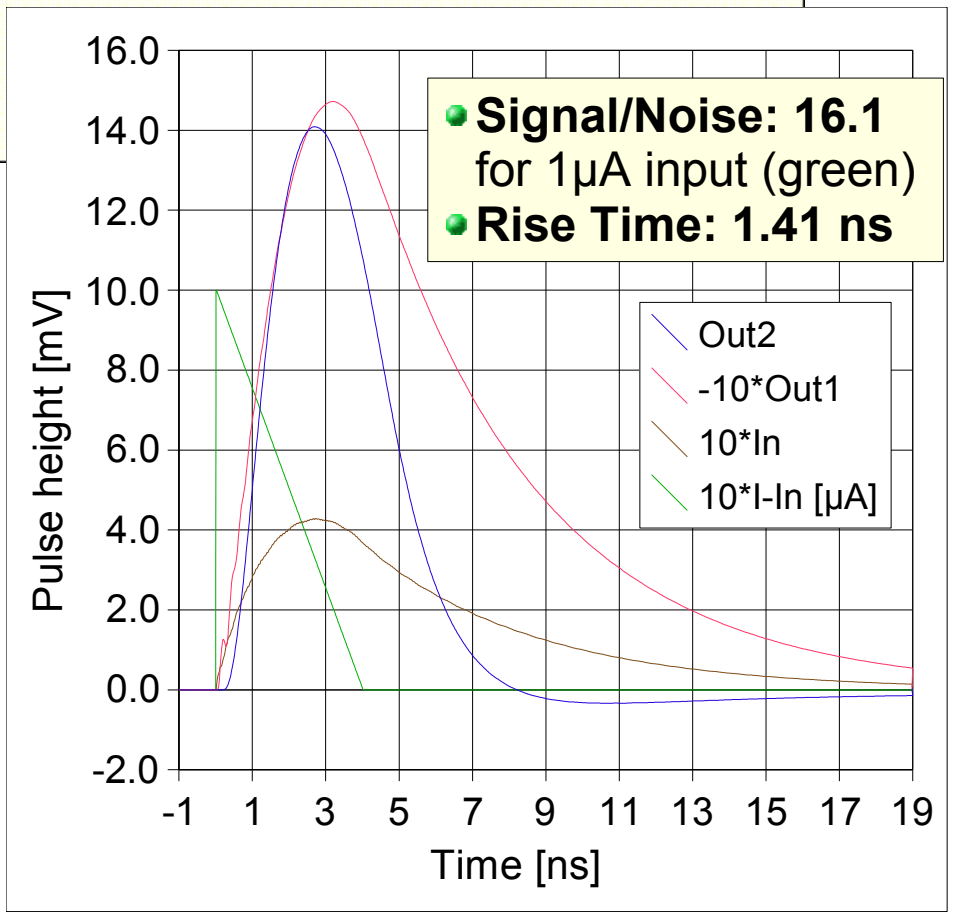
Schematics including 'virtual' components



Booster Amplifier, external

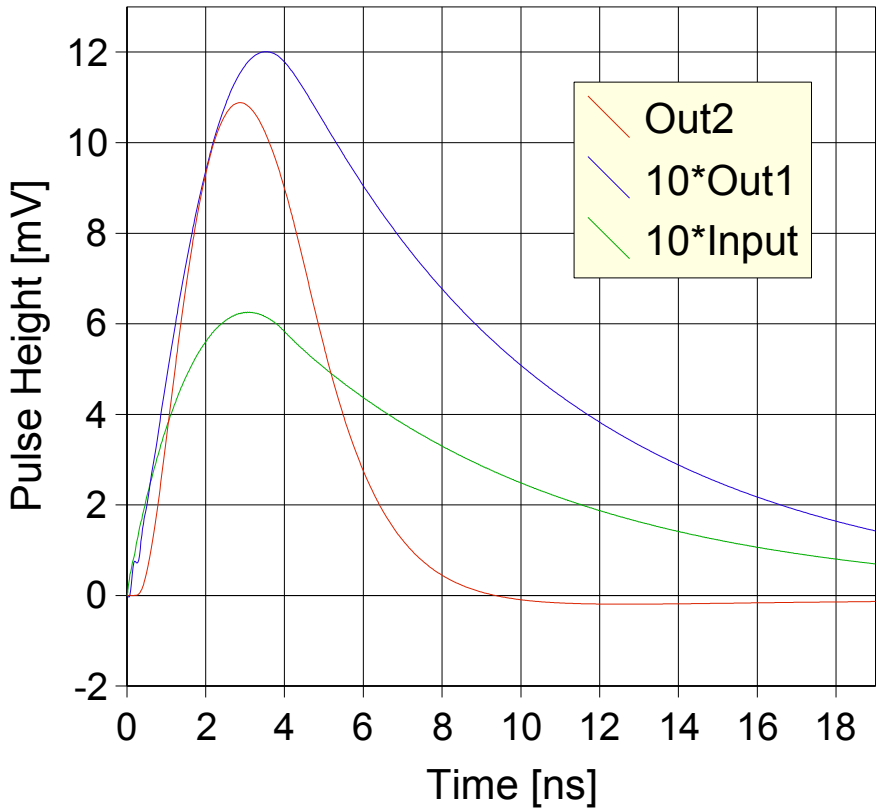
Noise Spectrum





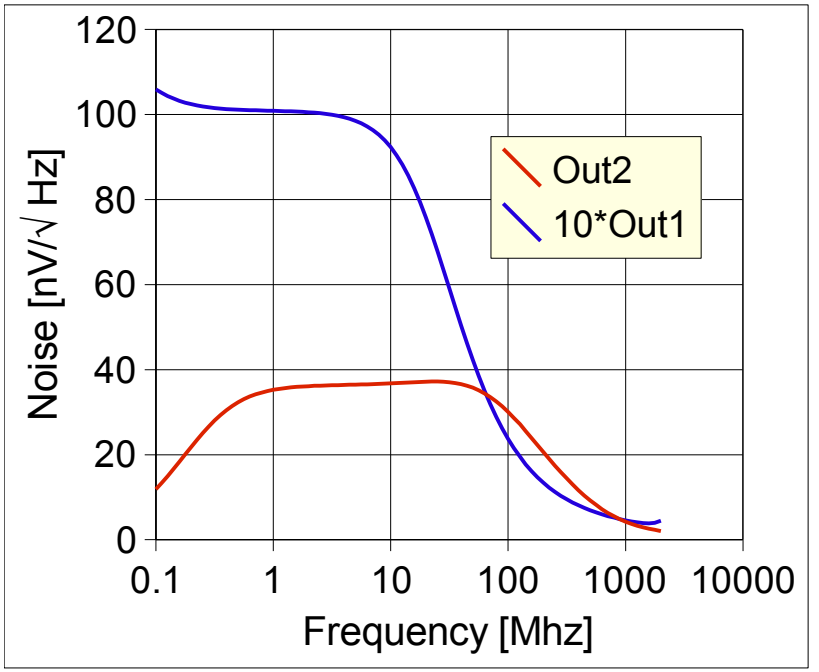
- **Signal/Noise: 16.1** for 1µA input (green)
- **Rise Time: 1.41 ns**

Signal/Noise can be optimized further (increasing risetime)



Pulse shapes before and after amplification

- Signal/Noise = 20.9 (1µA peak input)
- Rise Time = 1.5 ns



Noise spectrum before (blue) and after shaping (red)

Input impedance and capacitance as function of collector current:

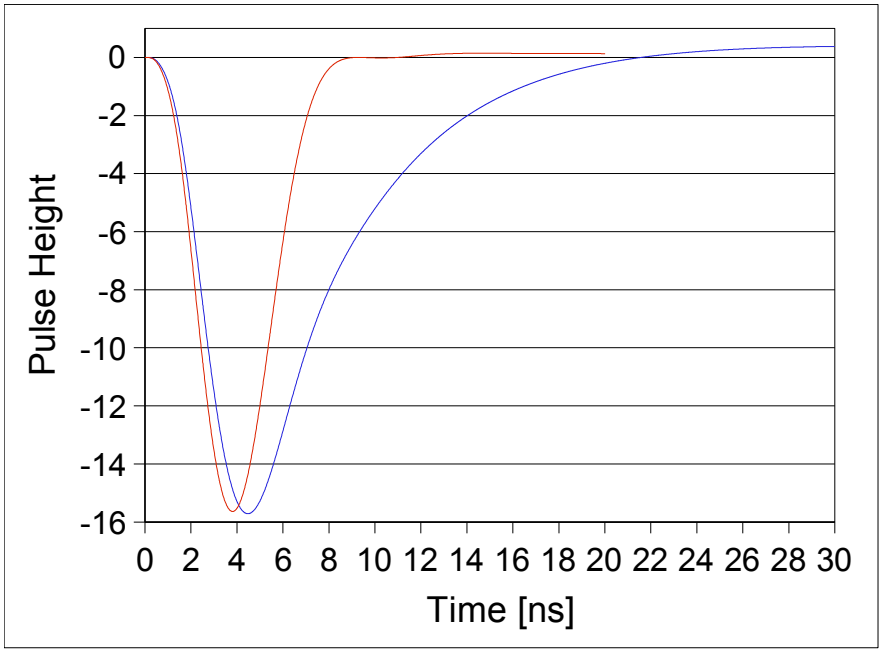
- 2.05 mA: 1.1 kΩ , 2.5 pF
- 0.93 mA: 2.3 kΩ , 2.1 pF

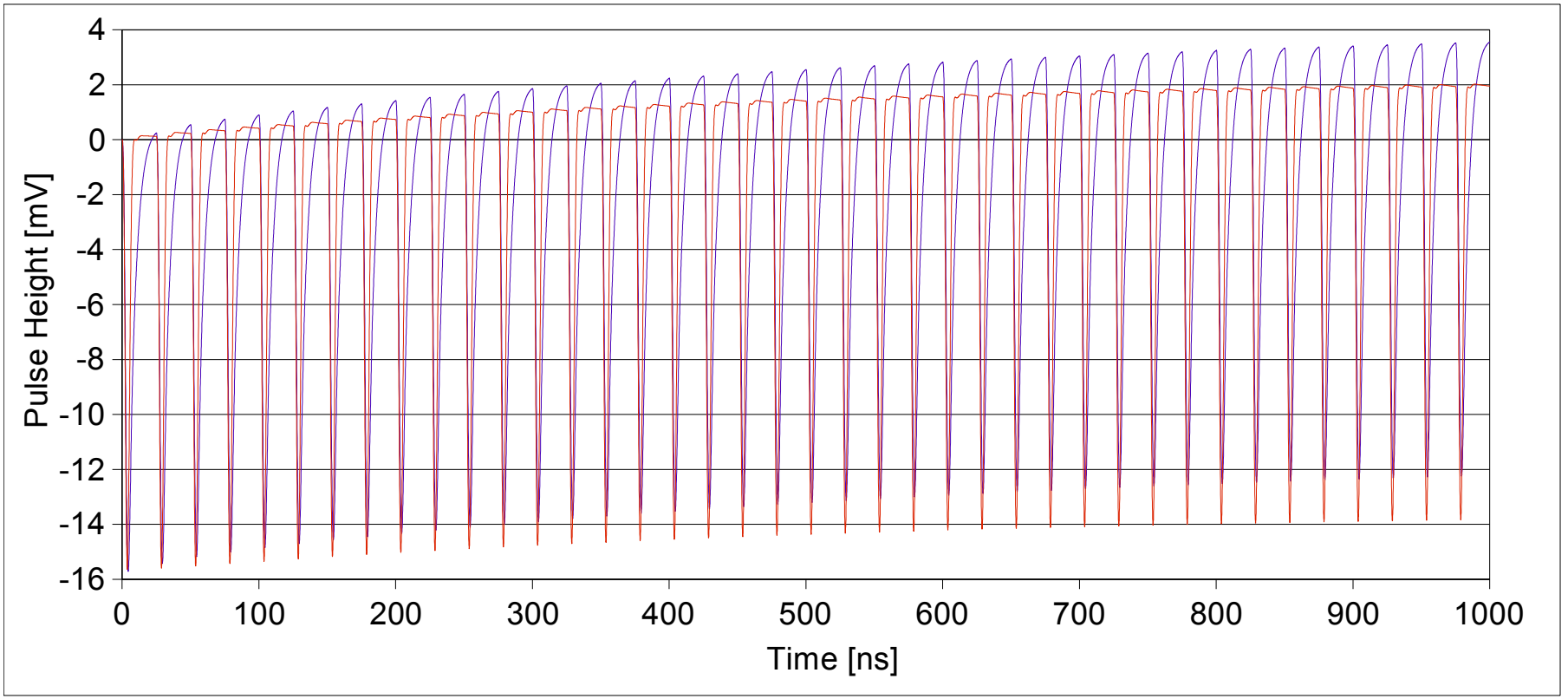
Large input capacitance due to feedback capacitance * Voltage gain

Baseline Shift

40 Mhz pulse frequency (25 ns repetition rate)

- Random rates do not cause baseline shifts (1 µs integration time
- no problem, if >95% effiency is required for random rates (< 6.5 MHz)

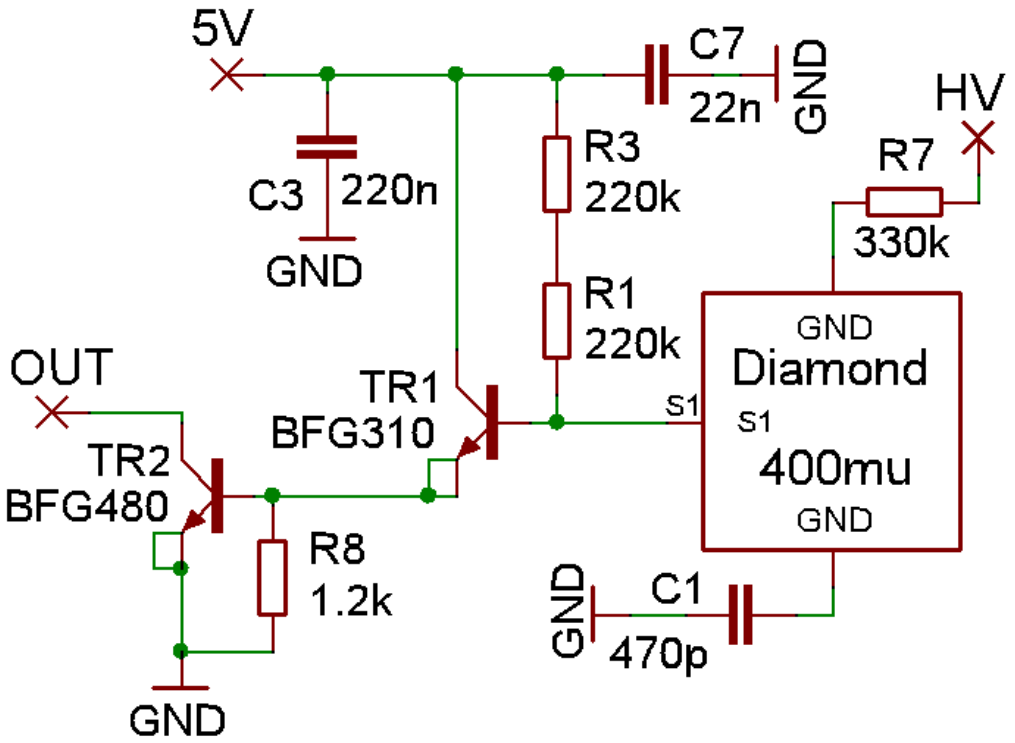


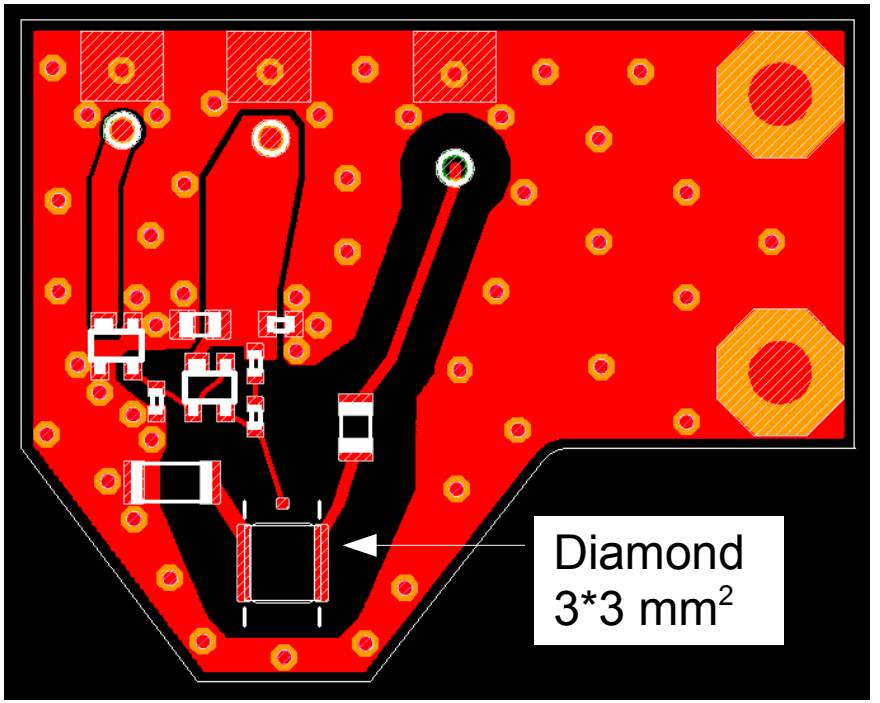


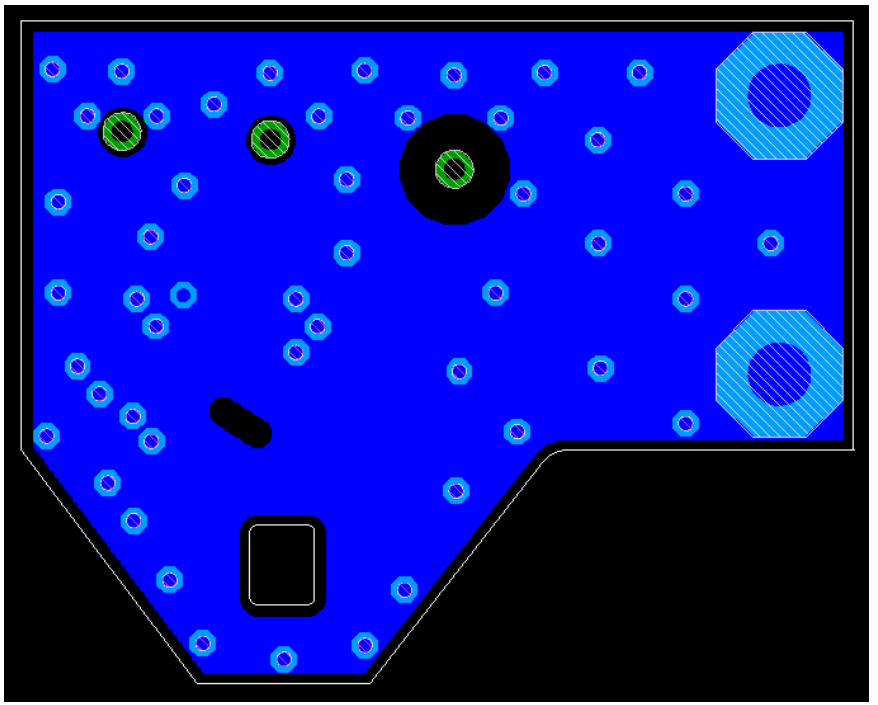
Diamond with a dual Transistor Amplifier

Optimize Signal / Noise further:

- High Impedance 1st stage (10 kOhm, 1.4 pF)
- Booster Transistor (25mA @ 2V, 50mW)
- Externally optimized signal shaping (high rates)





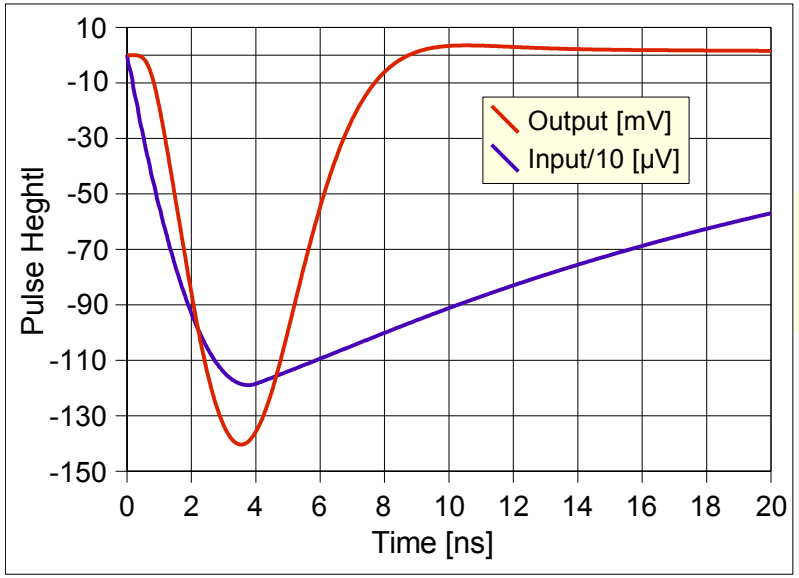


Schematics (above) and possible Layout (right)

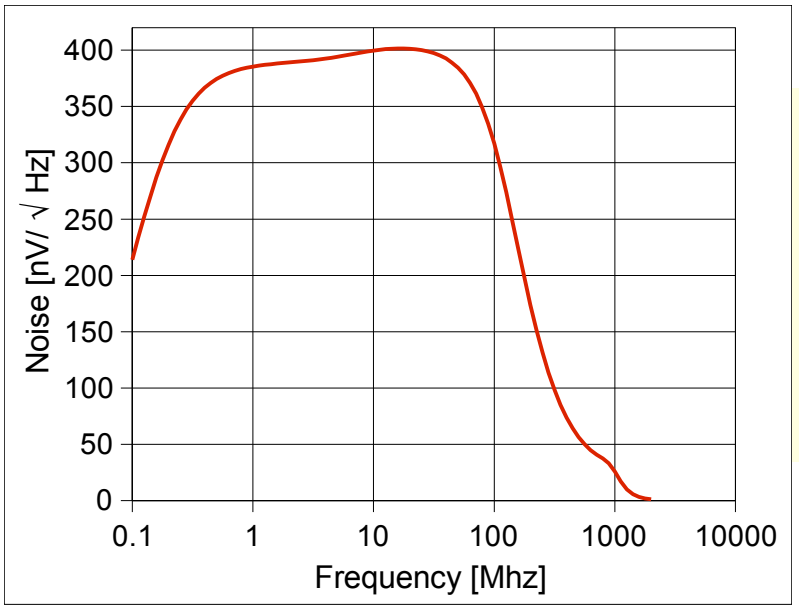
Large Filter Capacitor & HV protection resistor serve all readout channels (segmented readout)

Additional Shaping via external Booster Stage (further signal shaping)

Signal/Noise = **28.7** (1µA peak current)
maximized random Rate



Repetition Rate: 1/8 ns = 125 MHz



Wide Noise Frequency Response (Unipolar Signal)

Rise Time:
1.85 ns 1.71ns

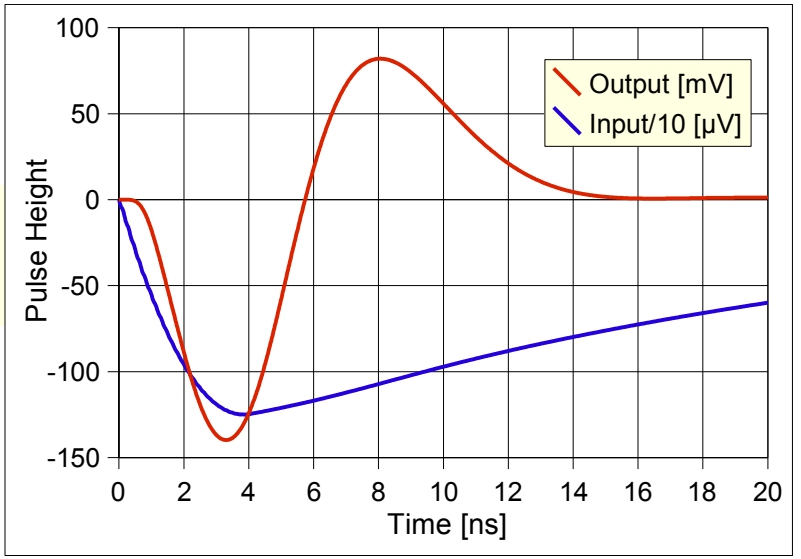
Linear, noise free amplifier:

- Signal / Noise:14

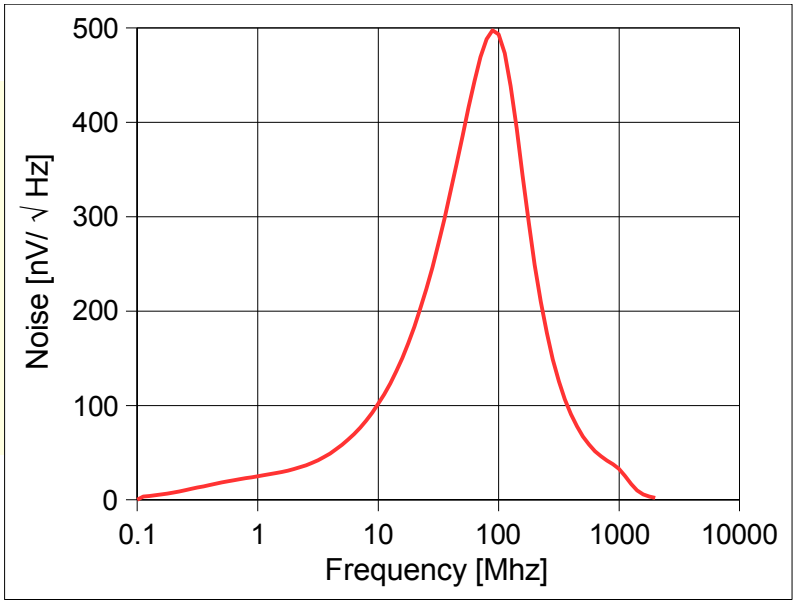
Shaping improves

- S/N by factor 2
- Rate by factor 3

Signal/Noise = **25.2** (1µA peak current)
minimized Baseline Shift



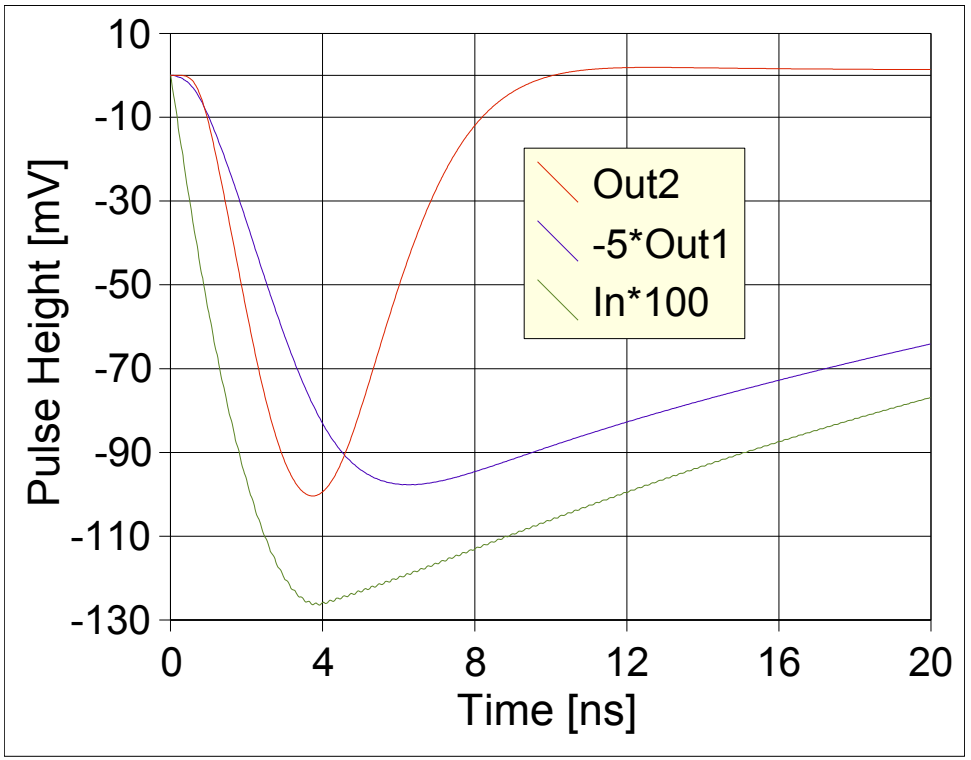
Repetition Rate: 1/12.5 ns = 80 MHz

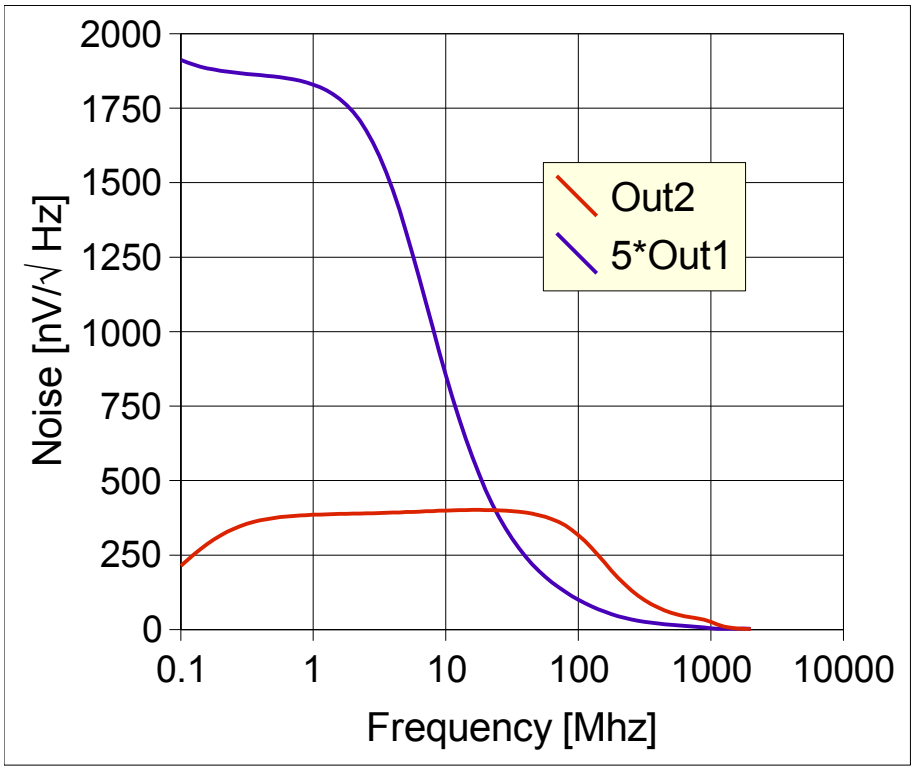


Narrow Noise Frequency Response(Bipolar Signal)

The best signal / noise ratio at a reasonable rise time

- Signal/Noise =33.6
- Rise Time = 1.94 ns
- 110 MHz (peak intensity/channel)





1st stage (Out1):
Integration over all electron/hole pairs
last stage(Out2): brute force shaping

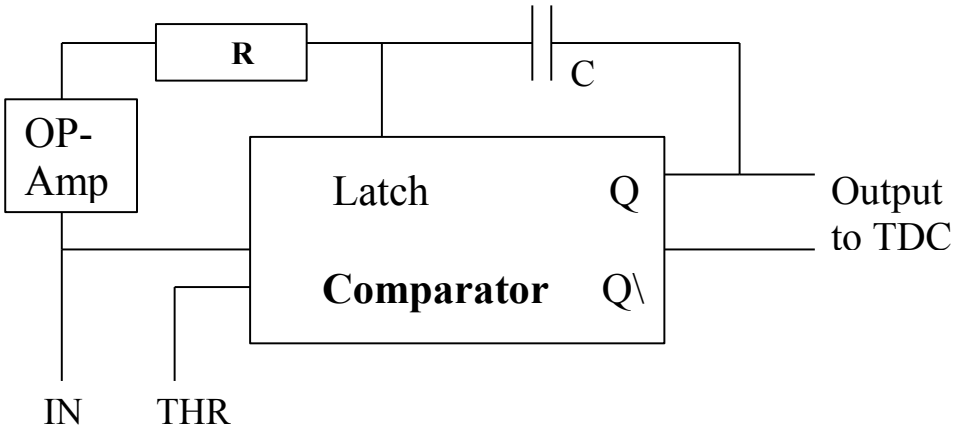
Shaping (Out2) removes low frequency noise (Out1)

Lower Limit on time resolution (ΔT / (S/N):

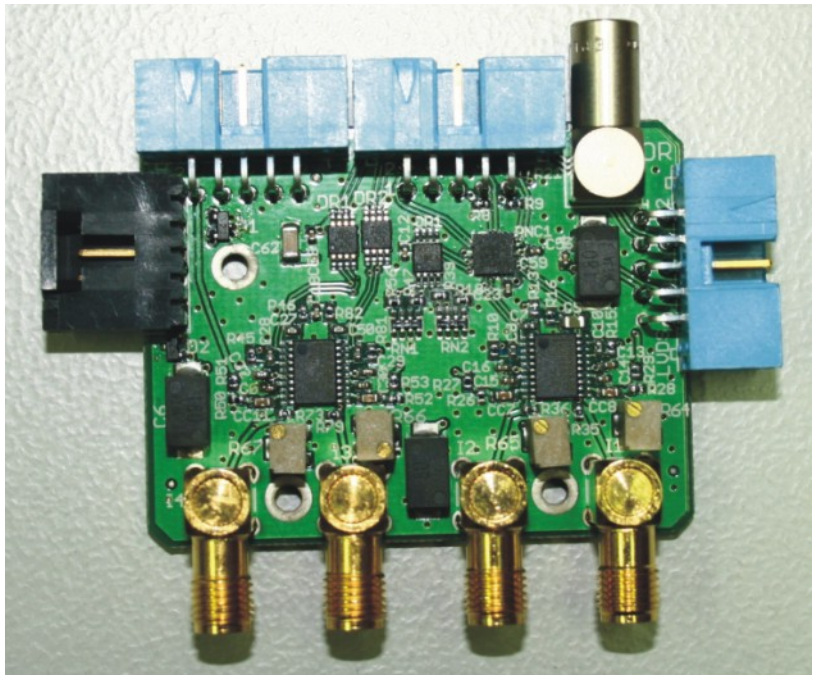
- one stage preamp: **75 ps**
- two stage preamp: **58 ps**

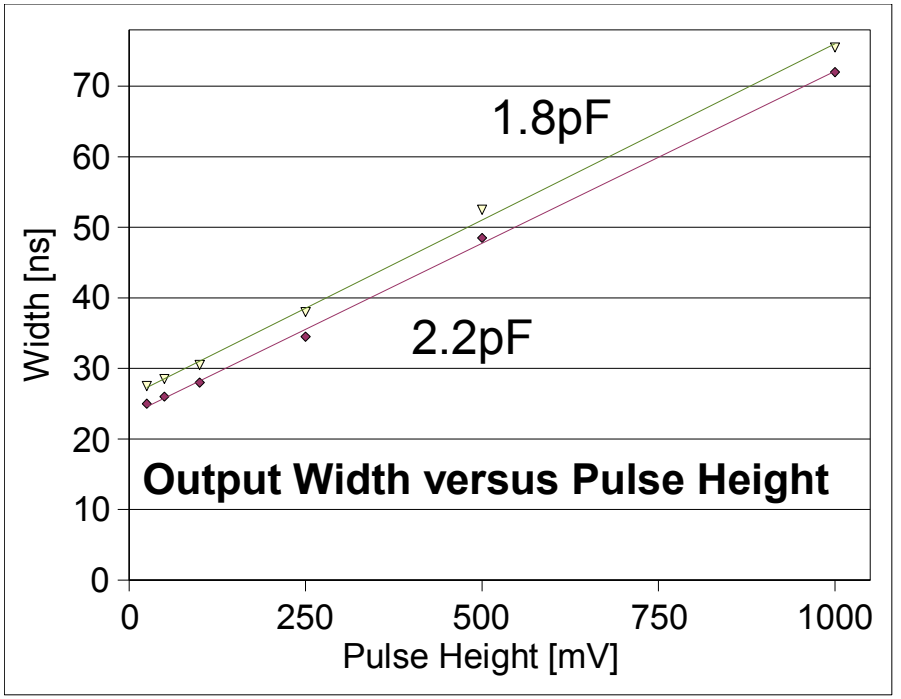
Leading Edge Discriminator

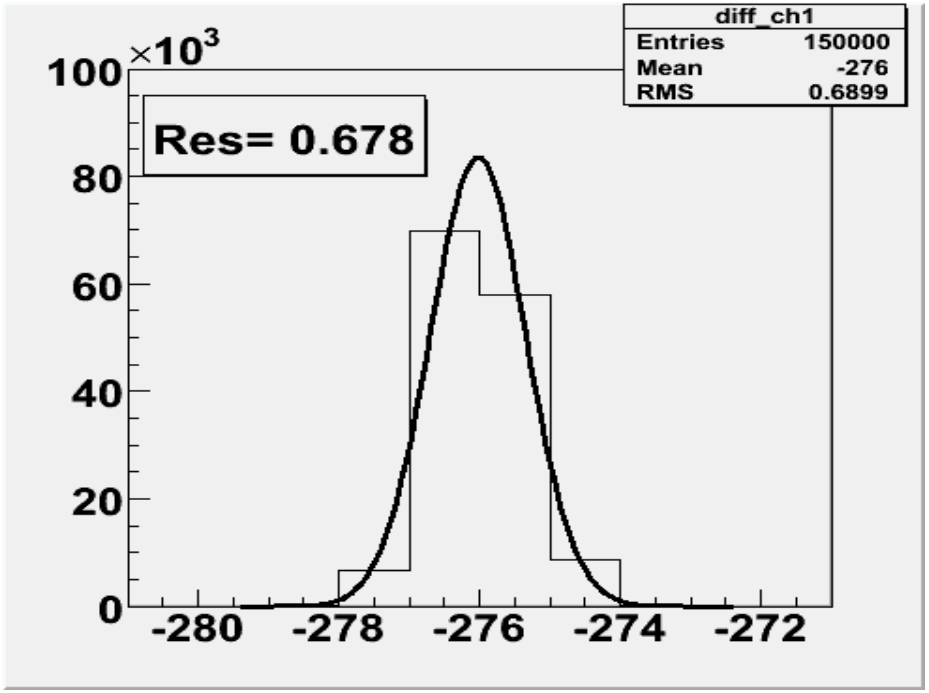
- Encode Charge in Pulse Width
- TDC measures leading and trailing edge
- No need for separate charge measurement



Schematic circuit for a simultaneous time and charge measurement (Max9601, 2GHz; Opa690,1.8V/ns)

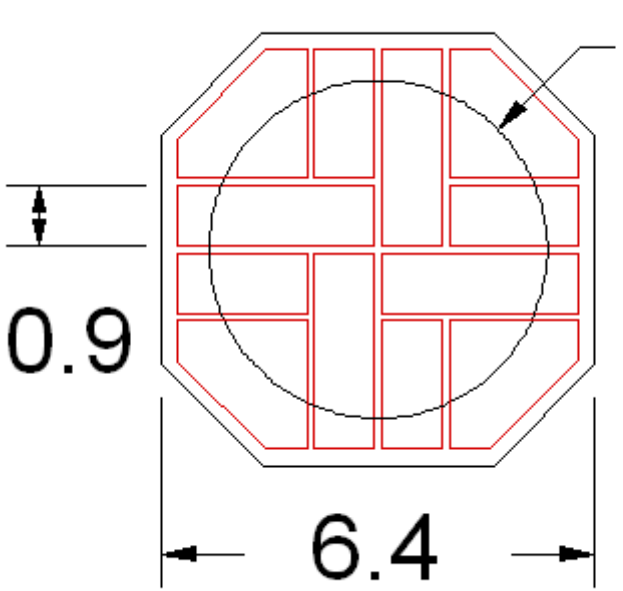




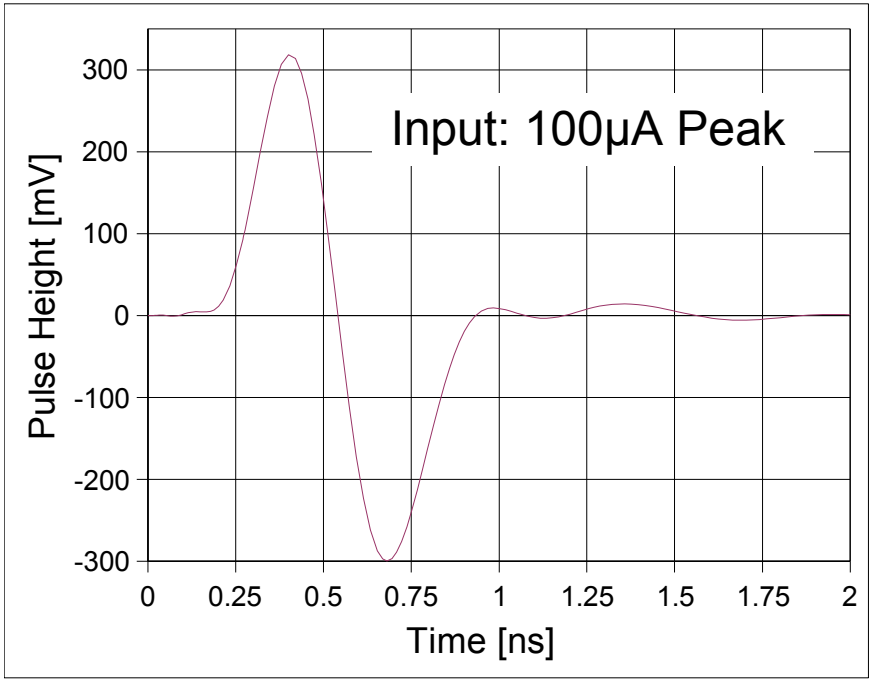


Trailing - Leading edge, Pulse Height = 80 mV
Resolution (70 ps) mainly determined by trailing edge

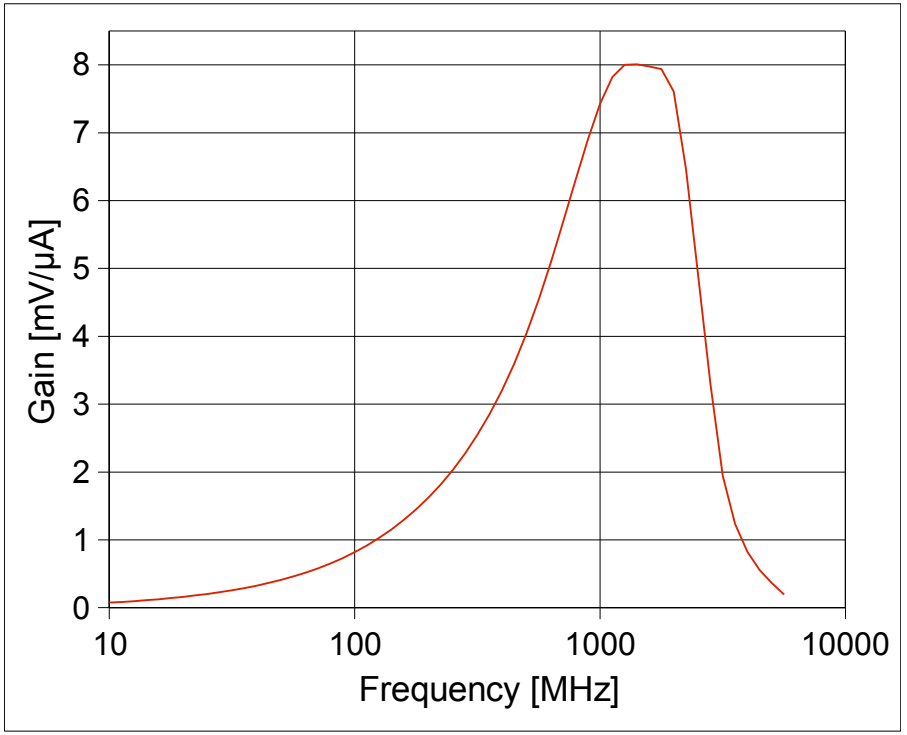
High Rate (10^9 random) Readout of a 12 fold segmented Diamond Detector(50µ)

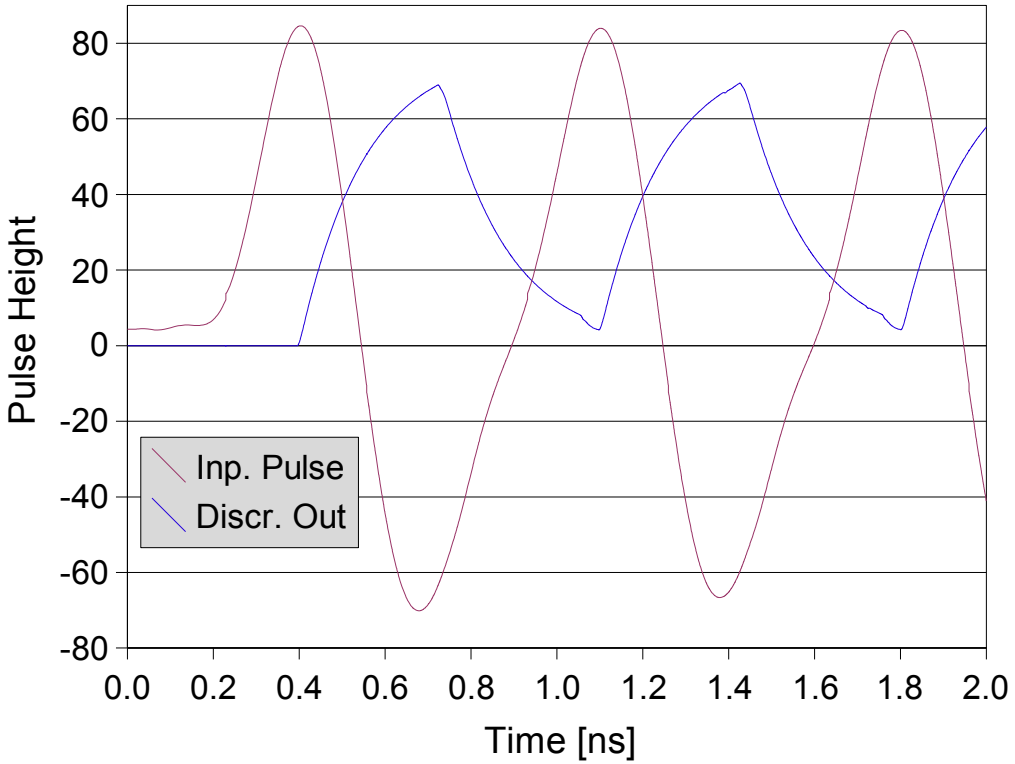


Delay Line shaped Signal
ΔT = 135ps
(Simulation)



Frequency Response





1.4 Ghz Pulse Frequency, Discr. Output scaled

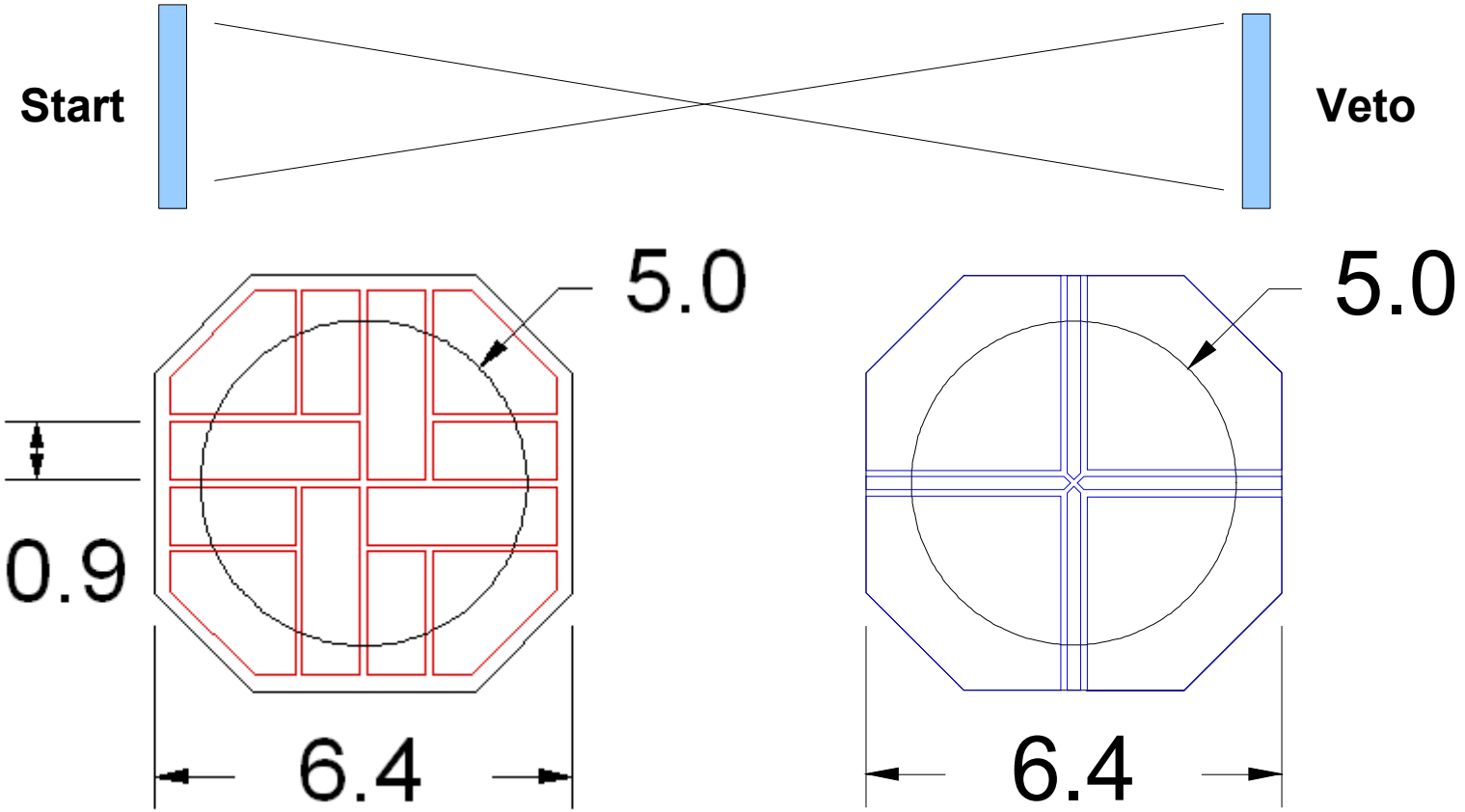
Monitoring requires Prescaler

MC100EP33 (4 GHz)

- downscale by factor 4
- derandomize

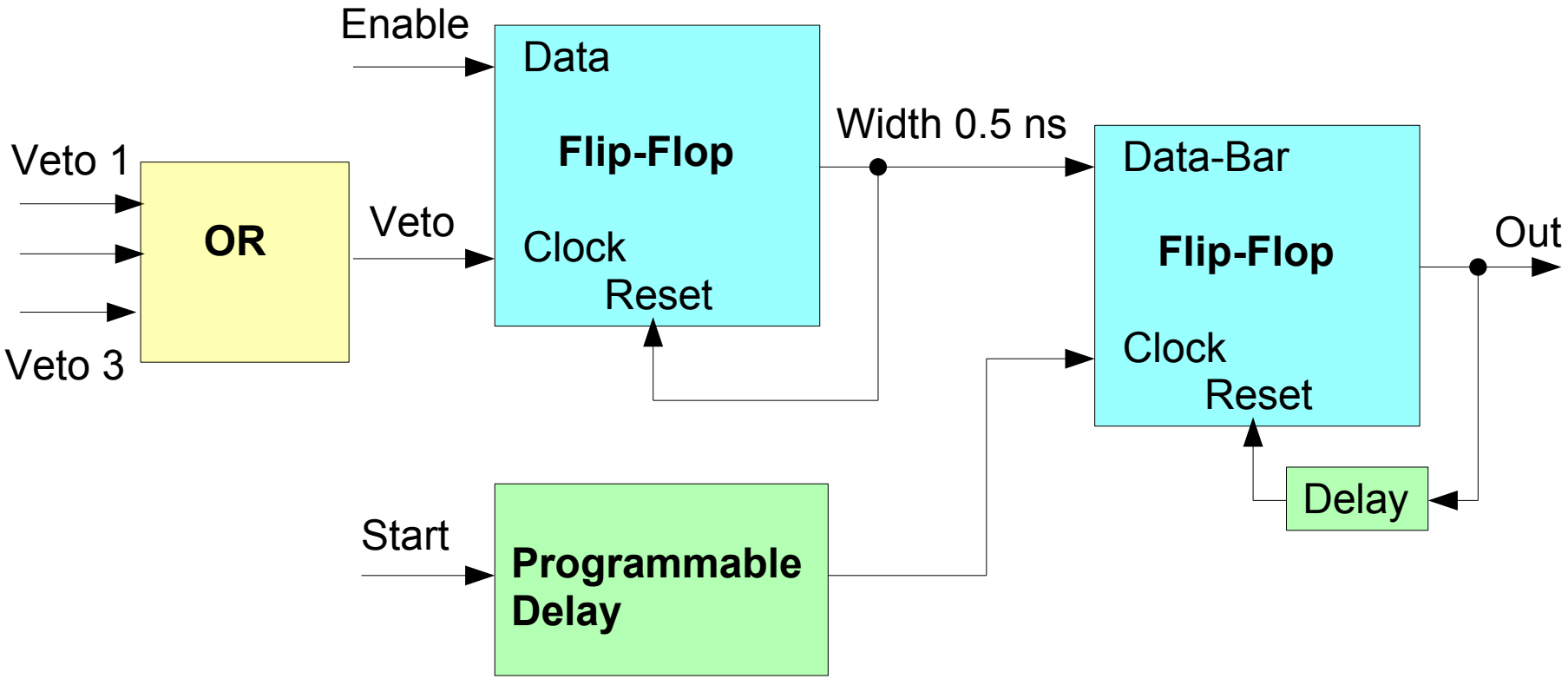
500 Mhz FPGA for monitoring (12 Scalers, VME Interface)

Veto Detector (reduces rate by factor > 20)



Anti Coincidence between opposite stripes and neighbored stripes on backside
Remaining rate: 2% of ion rate.

Start – Veto Anticoincidence (Reaction Trigger, Timing Signal)

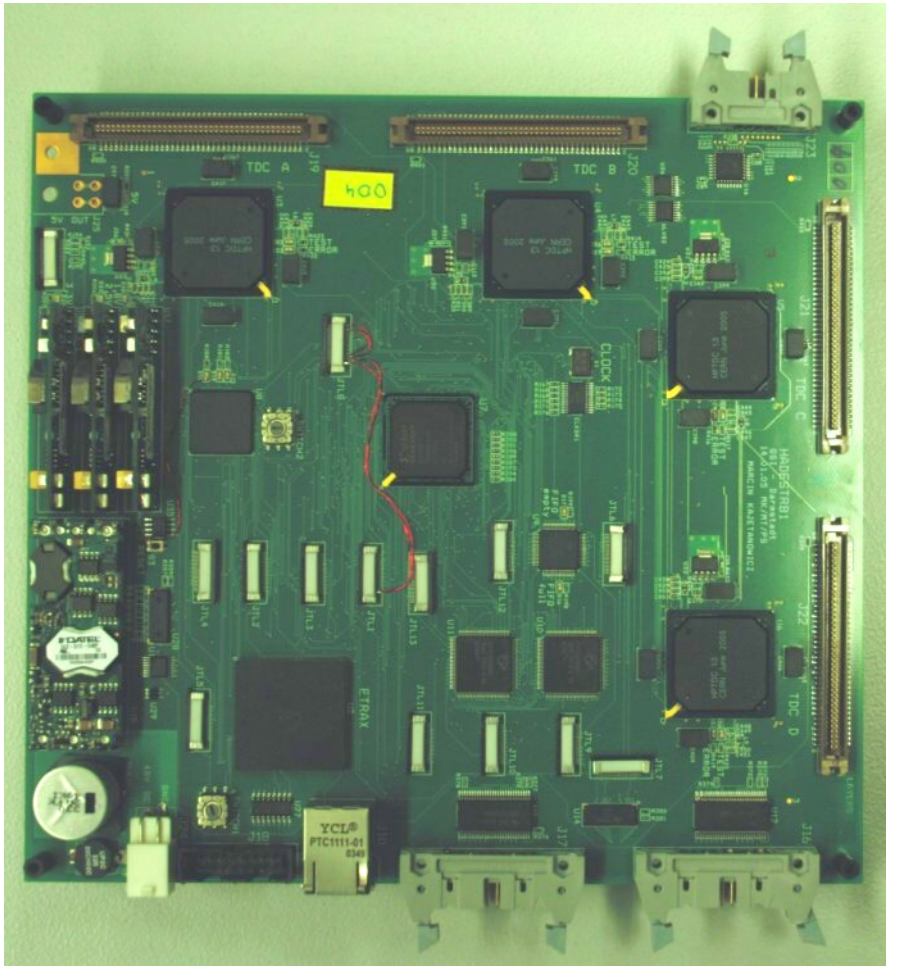


- Discrete Components (PECL) or FPGA (Virtex5)/ CPLD(MachX0)
- Integrated FPGA/CPLD solution currently not fast enough ?
- Discrete Solution available (Width = 2 -12 ns)

The Hades TRB Board (TDC)

- 128 Channels, Multi Hit, Leading Trailing edge
- Standalone Board (Linux PC, 100 Mb Ethernet)
- Single 48V Supply
- 1st, 2nd level (delayed) Trigger Handling
- Test Pulse outputs, DAC Threshold controls
- Scalable (Switch 10 * 100Mb In, Gb Out -> PC)

- 100 ps binning (25ps,32 channels)
- Resolution 29ps (measured for 100ps binning)
- Adjustable Time Window, no Delays needed
- max 80 kEvents/s 1st Level rate
- 2nd Level: 1.5MB/s $\rightarrow$ 10MB/s (next version)
- Software controlled data formatting



M. Traxler, M. Kajetanowicz, M. Palka, R. Trebacz

Summary

- MMICS provide Signal/Noise close to the theoretical limit.
- Placing 1st stage amplifier close to detector improves signal/noise.
- Charge integrating amplifiers (at Detector) with optimized (external) shaping might allow to measure MIPS at high rates (>120 Mhz Peak) with good time resolution (<100 ps).
- Discriminator / TDC combination allows charge (Pulse height) measurements without additional circuitry.
- 10 Ghz (Peak intensity) Start-Veto Diamonds seem to be feasible regarding the full readout chain.

Acknowledgment

GSI EE-Department in particular:
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