PADI, a new ASIC for RPC's 
RPC's and other timing detectors 
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Outline

• Introduction to timing measurements
• Simulations
• Integrated circuits\(^{(\text{FEE3})}\) vs Custom chip\(^{(\text{NINO2})}\)
• DESIGN of PADI ASIC, starting from NINO1
• Comparison: PADI versus NINO1
  a) Time over Threshold behavior
  b) Timing performance
• Summary and Outlook
Basic components of a timing measurement

If $\sigma_n \sim \sqrt{Nd \cdot BW}$
$dV/dt \sim As/t_r$
$t_r = 0.35/BW$

then

$\sigma_t \sim \sqrt{Nd / As \cdot \sqrt{BW}}$

Typical Errors

"WALK"

"JITTER"

\[
\sigma_t = \frac{\sigma_n}{dV/dt \mid V_{THR}}
\]

\[
\sigma_t = \frac{\sigma_n}{dV/dt \mid V_{THR}} + \delta t
\]
"Walk" and Sigma versus: UINP, Amplifier BW, Detector Rise Time
Detector signal is Step with variable Rise Time, Noise=3uV, THR=100mV
"Walk" and Sigma versus: UINP, Amplifier BW, Detector Rise Time
Detector signal is Step with variable Rise Time

**"WALK" [ns]**

- Circle: 10ps
- Square: 100ps
- Diamond: 1ns
- Triangle: 10ns

**Sigma [ps]**

- Blue: 35MHz
- Green: 350MHz
- Red: 3.5GHz
- Black: 35GHz

**Amplifier BW**

- 35MHz
- 350MHz
- 3.5GHz
- 35GHz
Sigma versus UINP and THRESHOLD for two Noise values

SIGMA [ns]
INPUT NOISE=24μV

SIGMA [ps]
INPUT NOISE=3μV

THRESHOLD
-20mV
-40mV
-60mV
-80mV
-100mV

UINP [mV]
Comparative Dependence to BW and Signal Rise Time for: Resistive Plate Chamber, PC and SC Diamonds

**Signal: Triangle, TR=TF**
- UINP=2mV
- UTHR=60mV

**Signal: Triangle, TF=1ns**

**Signal: Trapez, 4ns, TR=TF**
- Signal : TR
- 30ps
- 100ps
- 300ps
- 1ns
Simulations with CADENCE for FEE-gain dependence

- **GAIN=200**
- **GAIN=100**
- **GAIN=50**
- **GAIN=25**

- **FOPI-threshold**
- **Un ~50-60 mV**

- **Input Noise = 24 uV**
FOPI Experimental Results

MRPC 19b 90cm-8Gaps-16Strips

Timing & Efficiency for four gain settings (77, 130, 160, 220) of FEE3 with FOPI MMRPCs. $U_{\text{thr}} \sim 80$ mV

Balance between electronic gain, detector gain and threshold.
**FEE3**
- 16 channels with discreet IC.
- Single ended 50 Ohms inputs, differential Time and Amplitude outputs.
- OR output
- Gain ~160 strong non-linear (stabilized LVDR).
- External: Threshold voltage, TEST E/D, LATCH E/D

**FEE-NINO**
- 16 channels with two NINO2 IC.
- Differential 100 Ohms inputs, differential Time outputs with Time over-Threshold modulation
- OR input and output
- External: Threshold voltage, TEST E/D
Combined Time Resolution of two channels:
Input signal is ~1.67mV or ~42fC

FEE-NINO + Tacquila2

\[ \sigma_t \approx 81\text{ps} \]

- Input signal: 500mV, 49.5dB attenuation
- Model: Gauss
- Equation: \( y = y_0 + \frac{A}{w \sqrt{\pi/2}} \exp\left(-2\left(\frac{x-x_c}{w}\right)^2\right) \)
- Weight: Keine Gewichtung
- \( \chi^2/\text{DoF} = 941.85509 \)
- \( R^2 = 0.96668 \)
- \( y_0 = 9.24361 \pm 10.32514 \)
- \( x_c = -0.44687 \pm 0.20375 \)
- \( w = 15.8987 \pm 0.64235 \)
- \( A = 8989.9025 \pm 474.79877 \)

FEE3 + Tacquila2

\[ \sigma_t \approx 34.3\text{ps} \]

- Input signal: 500mV, 49.5dB attenuation
- Model: Gauss
- Equation: \( y = y_0 + \frac{A}{w \sqrt{\pi/2}} \exp\left(-2\left(\frac{x-x_c}{w}\right)^2\right) \)
- Weight: Keine Gewichtung
- \( \chi^2/\text{DoF} = 414.95271 \)
- \( R^2 = 0.99758 \)
- \( y_0 = 2.75995 \pm 5.85003 \)
- \( x_c = -0.23004 \pm 0.03568 \)
- \( w = 6.72485 \pm 0.08715 \)
- \( A = 9372.27574 \pm 135.48564 \)
Combined Timing Resolution with TACQUILA 2

Comparison FEE_NINO versus FEE3
One channel Timing Resolution

- **FOPI 8-gap counters 50 Ω**
- **ALICE 10-gap counters 100 Ω**

- **FEE_NINO, No.1, Ch1+Ch3+Taquila2**
- **FEE3, No.4, Ch1+Ch3+Taquila2, THR=61 mV**

![Graph showing comparison of FEE_NINO and FEE3 with TACQUILA 2](image)

Sigma [ps] vs. UINPUT [mV]
About Technology: CMOS: AMS 0.35um or UMC 0.18um?

(AMS – Austria Mikro Systeme International, UMC – United Microelectronics Corp.)

Low noise charge amplifiers in submicron CMOS
P.O'Connor, J.-F.Pratte, G.De Geronimo
Vth International Meeting on FEE, 2003

Development of a Front-End ASIC for TEGS TPC
G.De Geronimo, Paul O'Connor, Veljko Radeka, Bo Yu
Vth International Meeting on FEE, 2003
NINO2 structure

IBM CMOS 0.25 um technology


Fig. 2. Schematic input stage of the NINO ASIC.

Fig. 3. Block diagram of the NINO ASIC.
Preamplifier: AC equivalent diagram
Discriminator: AC equivalent diagram
## AC simulations

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<tbody>
<tr>
<td><strong>Preamplifier</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>Low pass corner</td>
<td>27</td>
<td>12</td>
<td>27</td>
<td>12</td>
<td>31.6</td>
<td>5.5</td>
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<tr>
<td>PA Out</td>
<td>48</td>
<td>420</td>
<td>48</td>
<td>360</td>
<td>51</td>
<td>120</td>
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<td><strong>Buffer</strong></td>
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<tr>
<td>Eout</td>
<td>-1.1</td>
<td>10000</td>
<td>-1.1</td>
<td>8800</td>
<td>-</td>
<td>-</td>
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<td><strong>Discriminator</strong></td>
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<tr>
<td>TOut, Hys=off</td>
<td>48.3</td>
<td>280</td>
<td>48.3</td>
<td>260</td>
<td>47</td>
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<th>Component</th>
<th>sch.</th>
<th>sch. with Cp.layout</th>
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<tr>
<td><strong>Noise on PADI Preamplifier:</strong></td>
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<tr>
<td>Simulation BW [MHz]</td>
<td>500</td>
<td>1000</td>
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<tr>
<td>Noise PA Out [mV RMS]</td>
<td>4.52</td>
<td>5.17</td>
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<td><strong>Noise on NINO1 Preamplifier sch.</strong></td>
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<td>Simulation BW [MHz]</td>
<td>500</td>
<td>1000</td>
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<tr>
<td>Noise PA Out [mV RMS]</td>
<td>3.83</td>
<td>3.91</td>
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Comparison on Delay Times
NINO versus PADI
Comparison on Time Resolution: NINO versus PADI

<table>
<thead>
<tr>
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<th>Time Resolution [ns]</th>
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<tr>
<td></td>
<td>-32mV</td>
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<td></td>
<td>-64mV</td>
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<td>-256mV</td>
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<td>-512mV</td>
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</tbody>
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![Graph comparing NINO and PADI time resolution](image)
Comparison

Time Resolution
PADI versus NINO

Time Resolution
QINP [fC]

NINO -32mV
NINO -64mV
NINO -128mV
NINO -256mV
NINO -512mV
PADI -32mV
PADI -64mV
PADI -128mV
PADI -256mV
PADI -512mV
The influence of Layout parasitic capacitances on Time Resolution

loss: ~30%
WALK Correction: Time over Threshold or Q measurement?

PADI

EOut Peak Amplitudes (ref: midpoint 0 V)

Vpk [mV]

ToT [ns]

Threshold Voltage
-32mV
-64mV
-128mV
-256mV
-512mV

Baseline Voltage
-21mV
-42mV
-84mV
-164mV
-244mV

PADI

EOut Peak Amplitudes (ref: baseline)

Vpk [mV]

QIN [fC]

PADI

Time over Threshold

QIN [fC]

QIN [fC]
WALK Correction: .... or Integrated Q measurement?

Integral for fixed time (15 ns)

Baseline correction before Integral for fixed time (15 ns)
PADI

NEW ASIC!

the prototype has only 3 channels
Preamplifier & Discriminator in
0.18\(\mu\)m CMOS technology
1.5x1.5mm\(^2\)
Summary

- FEE3 vs FEE-NINO
  Due to the full differential structure, FEE-NINO has a lower sensitivity to pick-up of parasitic signals. To use all benefits of this design, the detector must be differential too.

Outlook

- We wait for first PADI chips for tests.
- The increase of PADI preamp/discriminator actual bandwidth is a hard task, but we will try to evaluate the limit of the used architecture.
- We will investigate the possibility to change the biasing type, from voltage to current, to decrease the crosstalk inside the PADI chip.
We acknowledge the support of the European Community-Research Infrastructure Activity under the FP6 "Structuring the European Research Area" programme (HadronPhysics, contract number RII3-CT-2004-506078).
Time over Threshold tests for FEE-NINO

FEE_NINO: Time over Threshold
Width of the output pulse, Input pulse is short triangle (1.8ns).

FEE_NINO: Time over Threshold
Width of the output pulse, Input pulse is step type.

Graph 1: UINP [mV] vs. OUTPULSE [ns] for various channels.
Graph 2: UINP [mV] vs. OUTPULSE [ns] for various channels.
Time Resolution measured with TDS 7104 Oscilloscope 1.3 GHz

Comparison FEE_NINO versus FEE3 Timing Resolution

Preliminary results