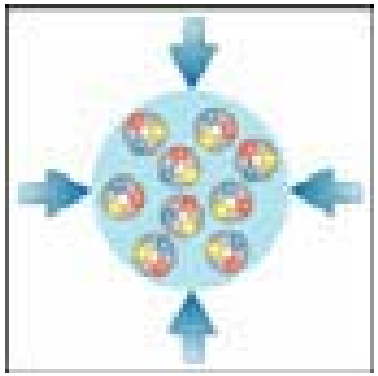
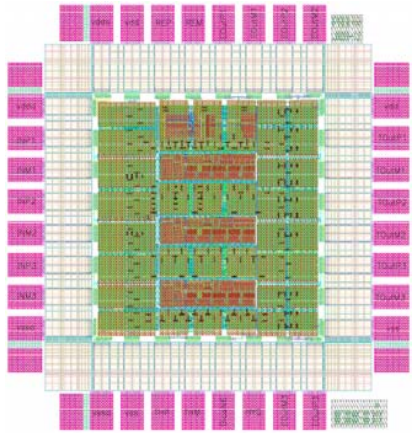
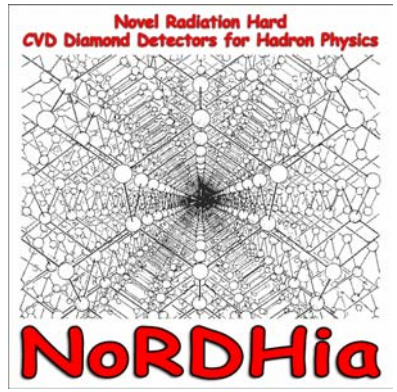






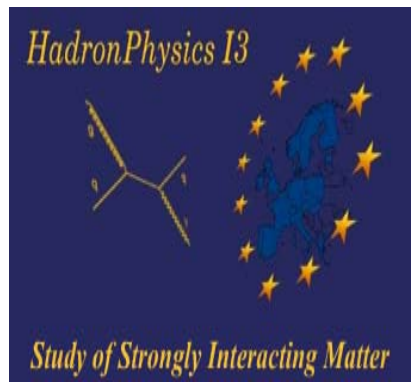
PADI, a new ASIC for RPC's
RPC's and other timing detectors

Mircea Ciobanu

NoRDHia Meeting

August 30-1 September 2006

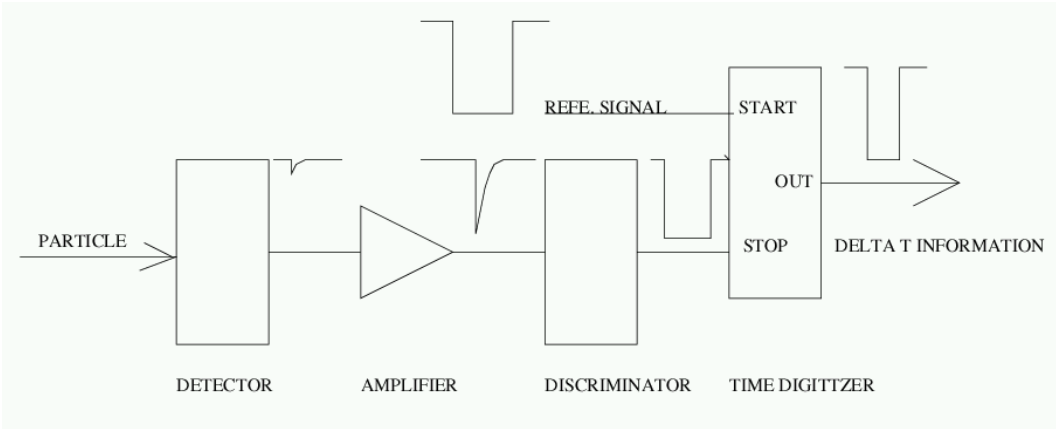
GSI-Darmstadt



Outline

- Introduction to timing measurements
- Simulations
- Integrated circuits(FEE3) vs Custom chip(NINO2)
- DESIGN of PADI ASIC, starting from NINO1
- Comparison: PADI versus NINO1
  a) Time over Threshold behavior
  b) Timing performance
- Summary and Outlook

Basic components of a timing measurement



if $\sigma_n \sim \sqrt{Nd*BW}$

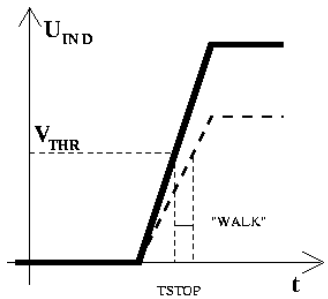
$dV/dt \sim As/t_r$

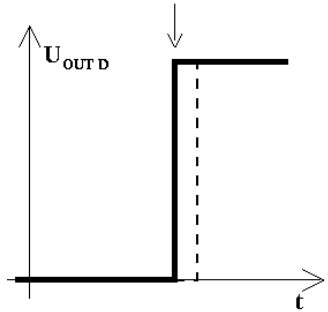
$t_r = 0.35/BW$

then

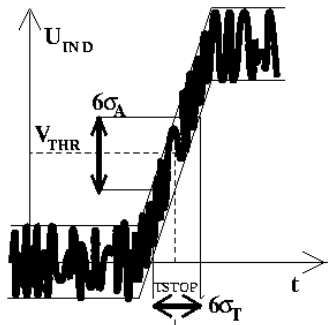
$$\sigma_t \sim \sqrt{Nd} / As\sqrt{BW}$$

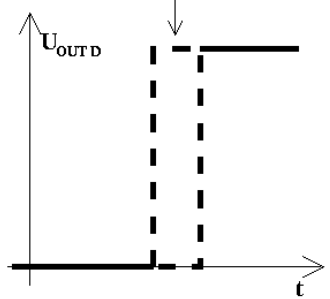
" WALK "





CLEAN SIGNAL APPLIED TO DISCRIMINATOR





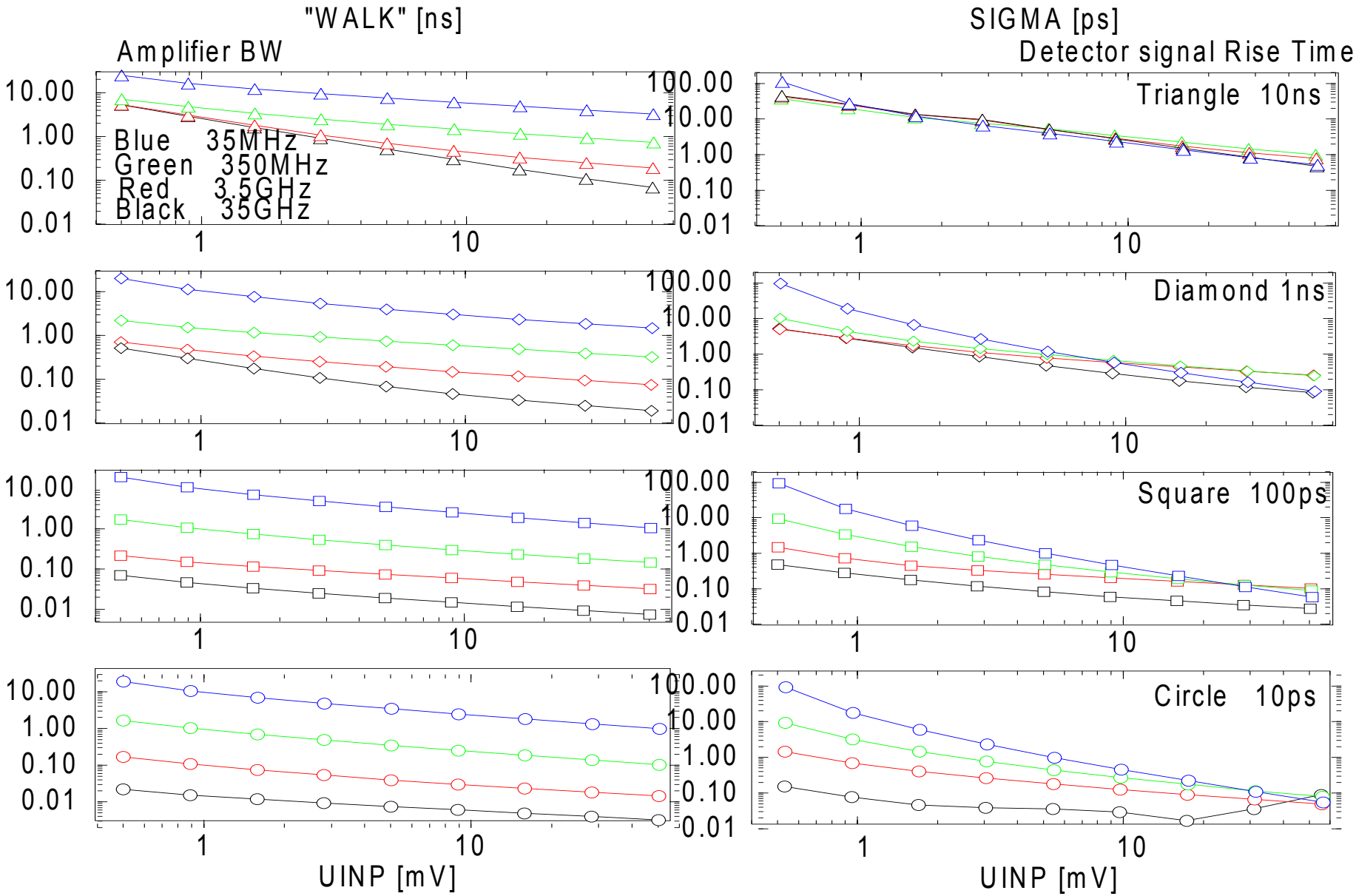
NOISY SIGNAL APPLIED TO DISCRIMINATOR

" JITTER"

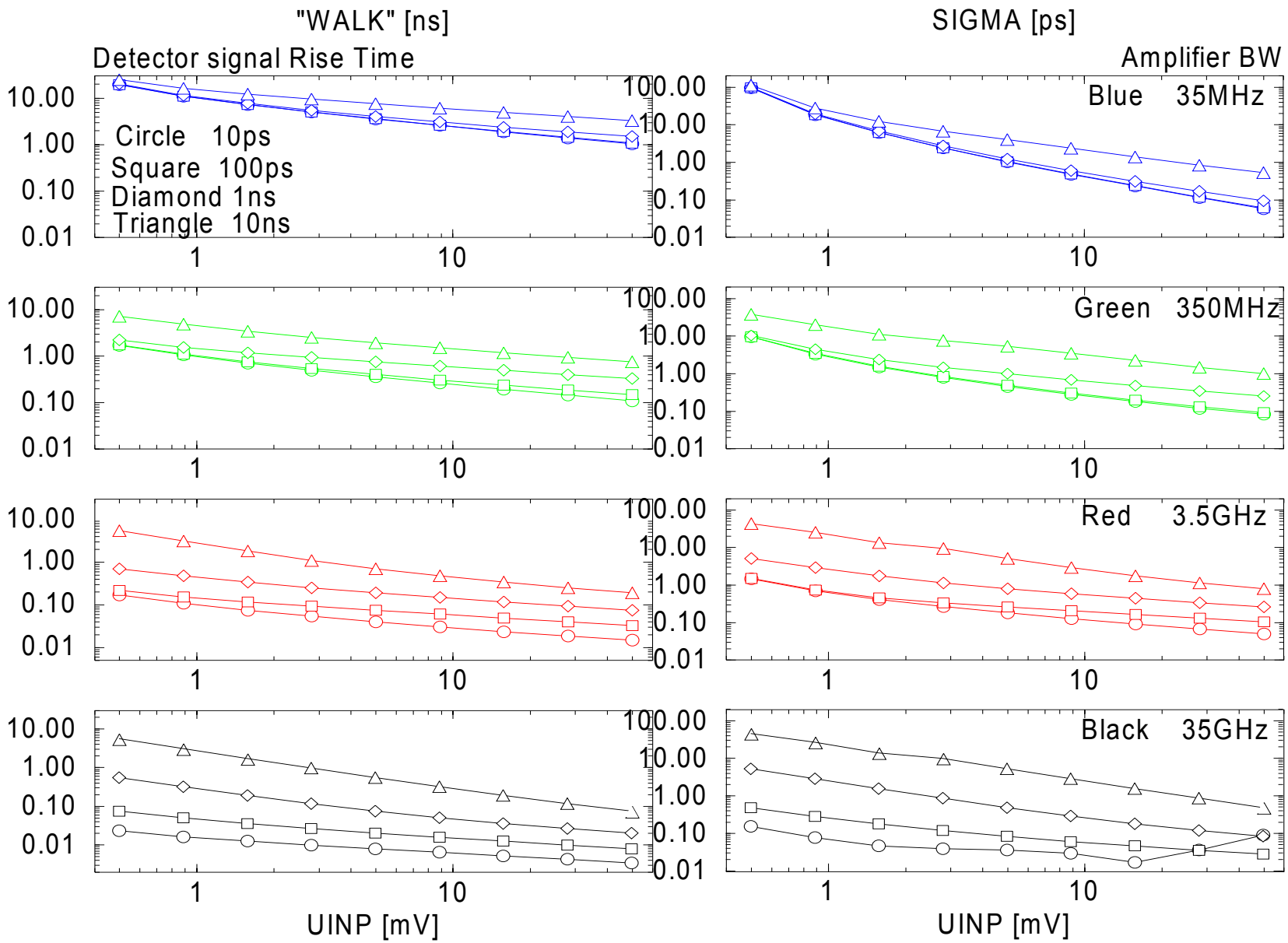
$$\sigma_t = \frac{\sigma_n}{\left.\frac{dV}{dt}\right|_{V_{THR}}}$$

$$\sigma_t = \frac{\sigma_n}{\left.\frac{dV}{dt}\right|_{V_{THR}}} + \delta t$$

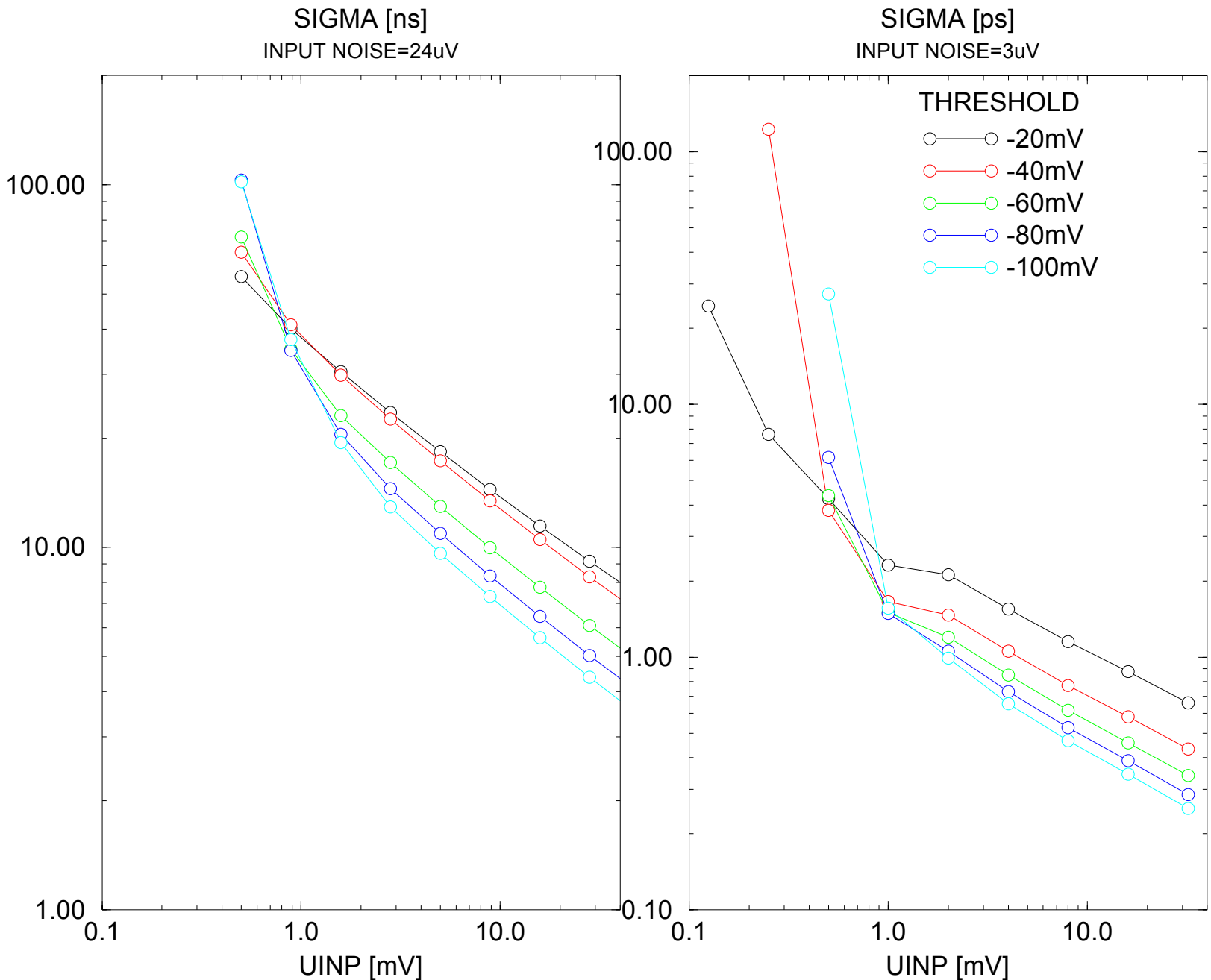
"Walk" and Sigma versus: UINP, Amplifier BW, Detector Rise Time
Detector signal is Step with variable Rise Time, Noise=3uV, THR=100mV



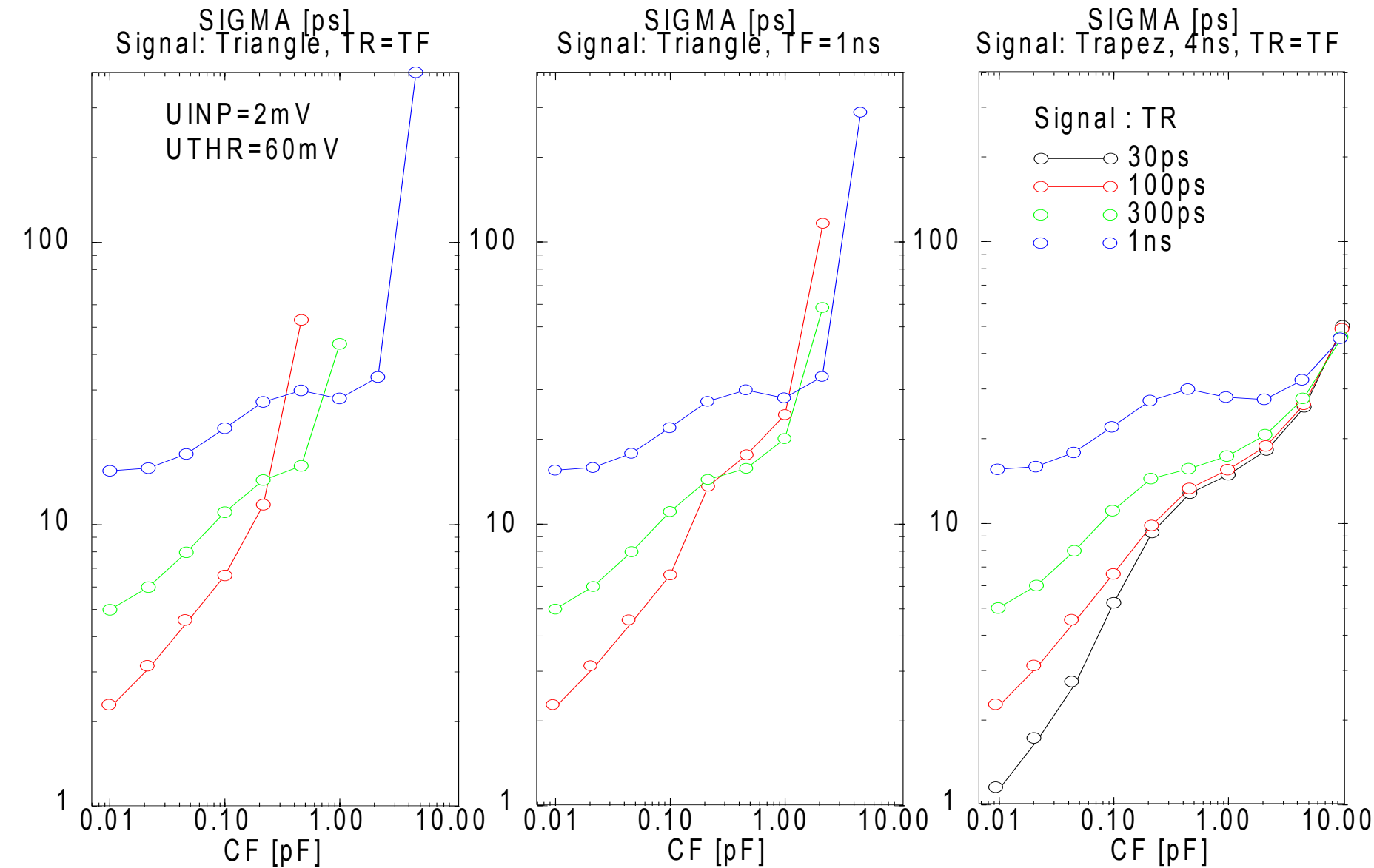
"Walk" and Sigma versus: UINP, Amplifier BW, Detector Rise Time Detector signal is Step with variable Rise Time



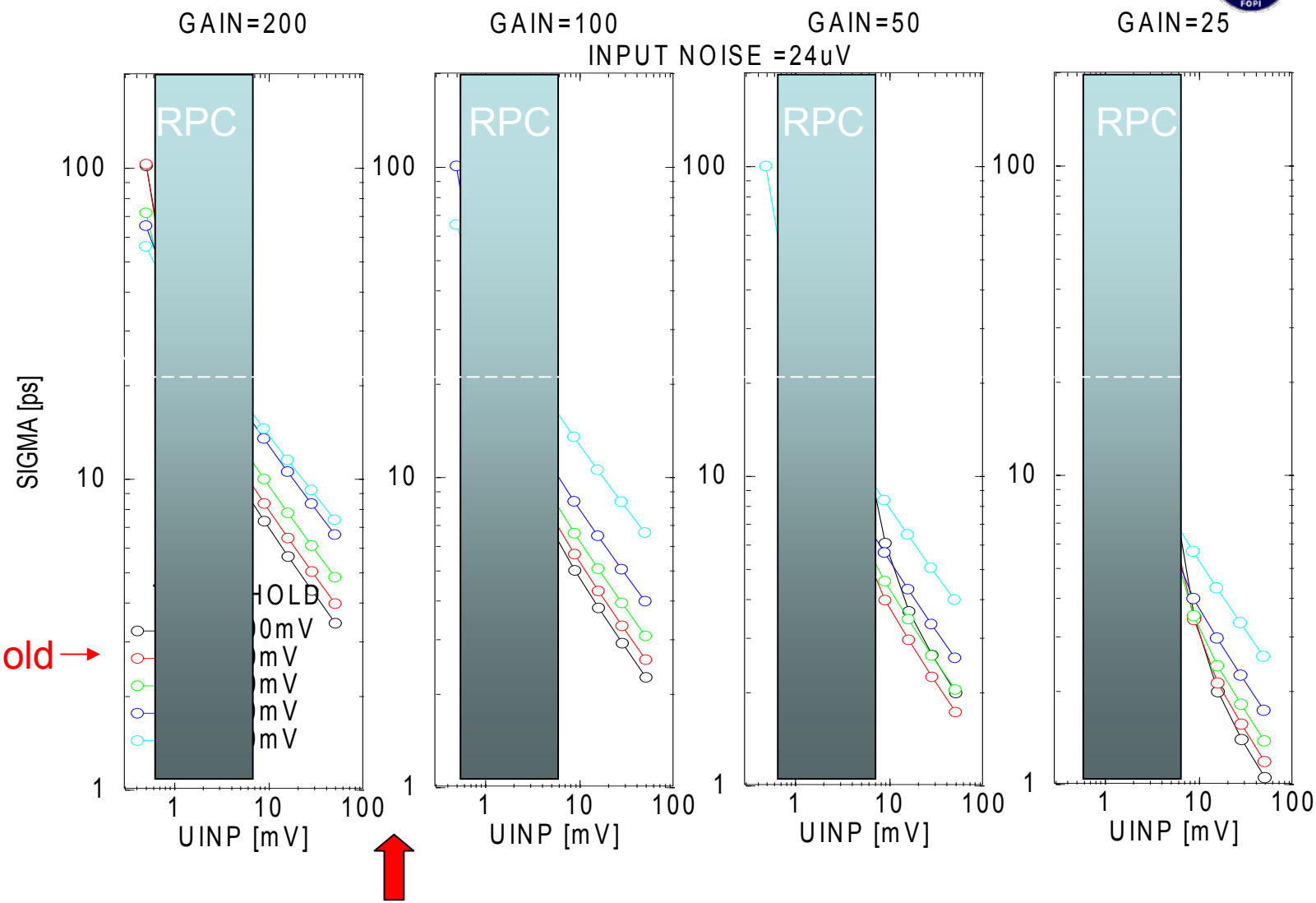
Sigma versus UINP and THRESHOLD for two Noise values



Comparative Dependence to BW and Signal Rise Time for : Resistive Plate Chamber, PC and SC Diamonds

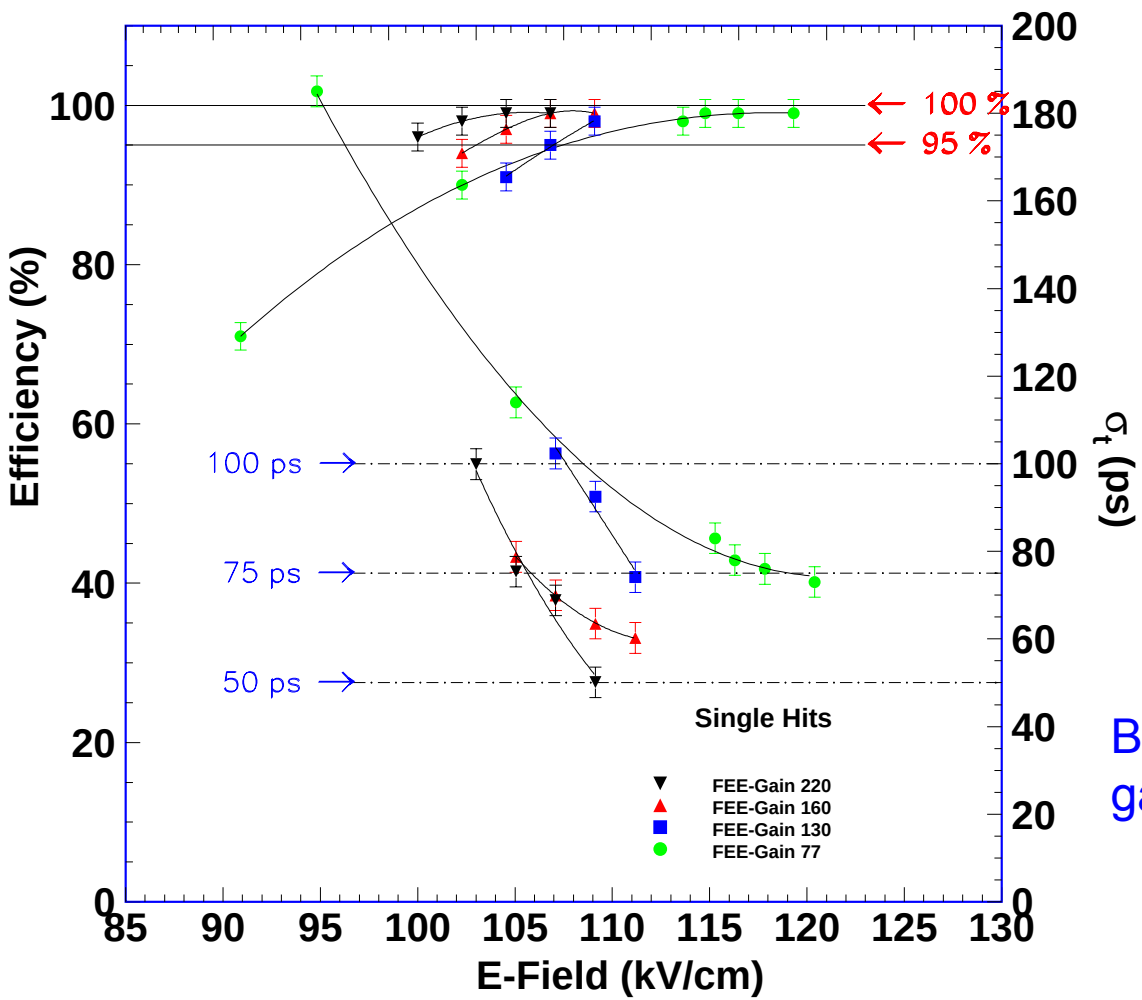


Simulations with CADENCE for FEE-gain dependence



FOPI-threshold →

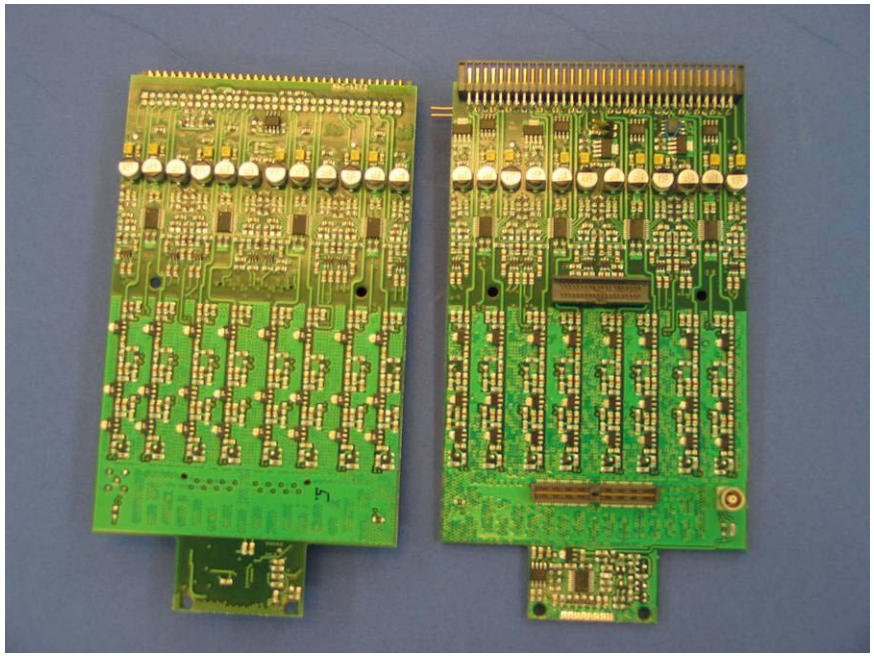
FOPI Experimental Results



Timing & Efficiency for four gain settings (77,130,160,220) of FEE3 with FOPI MMRPCs. U_{thr} ~80 mV

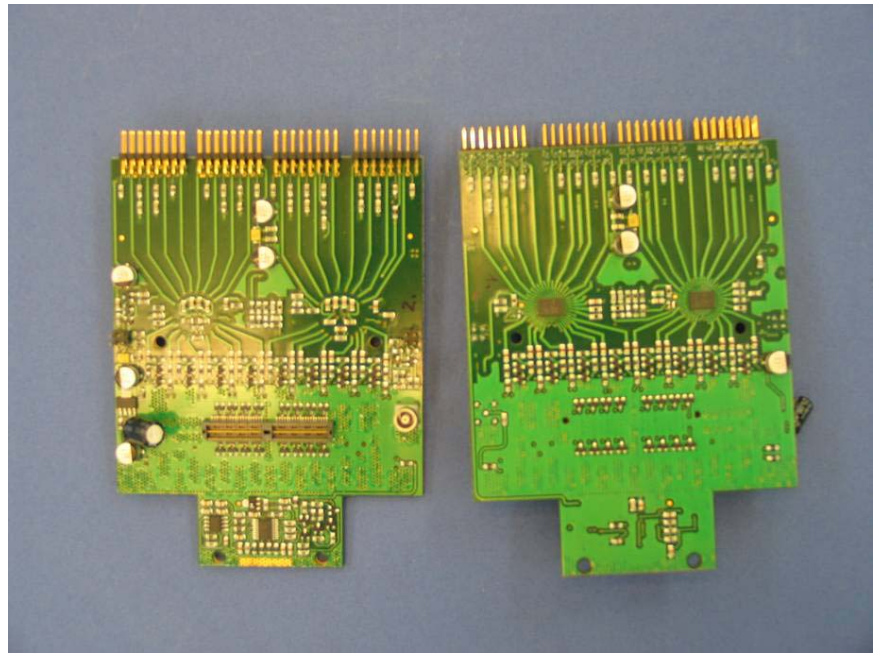
Balance between electronic gain, detector gain and threshold.

FEE3



- 16 channels with discreet IC.
- Single ended 50 Ohms inputs, differential Time and Amplitude outputs.
- OR output
- Gain ~160 strong non-linear (stabilized LVDR).
- External: Threshold voltage, TEST E/D, LATCH E/D

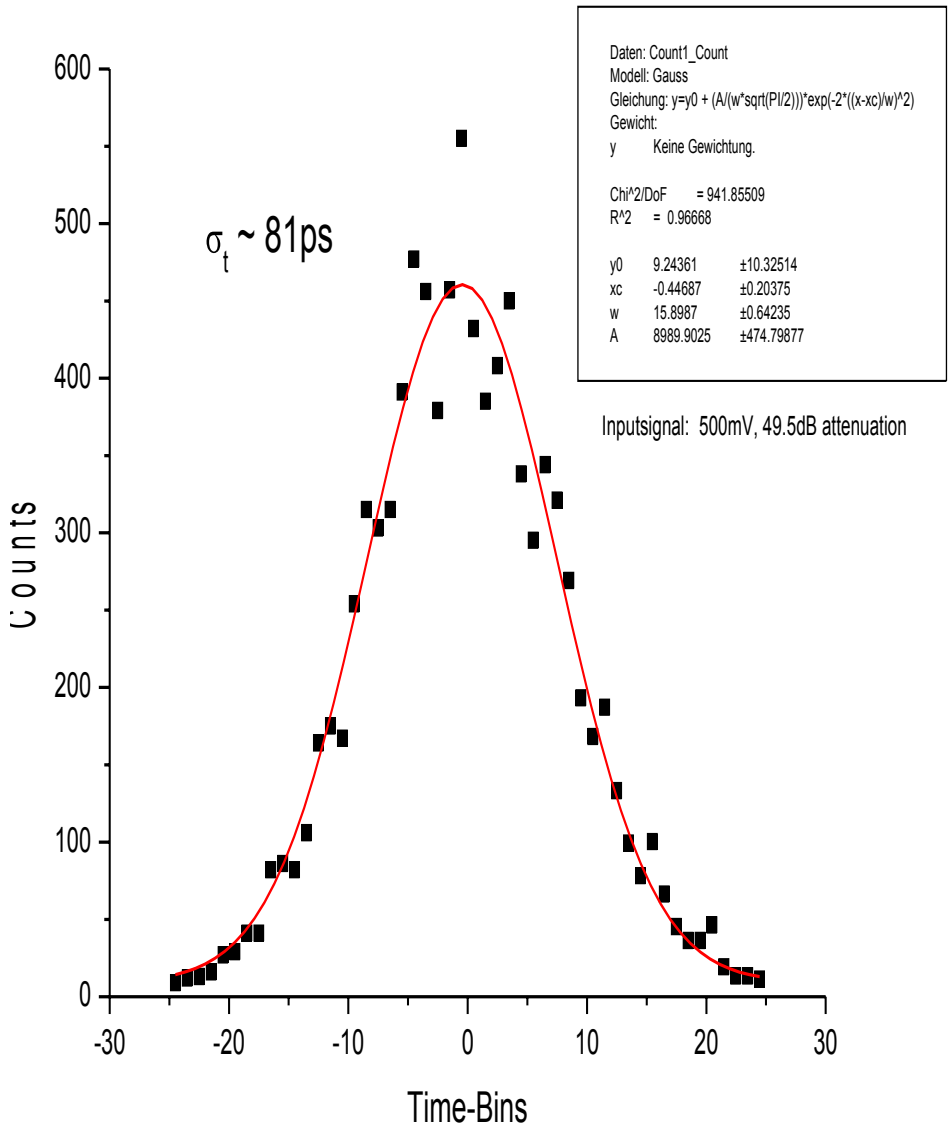
FEE-NINO



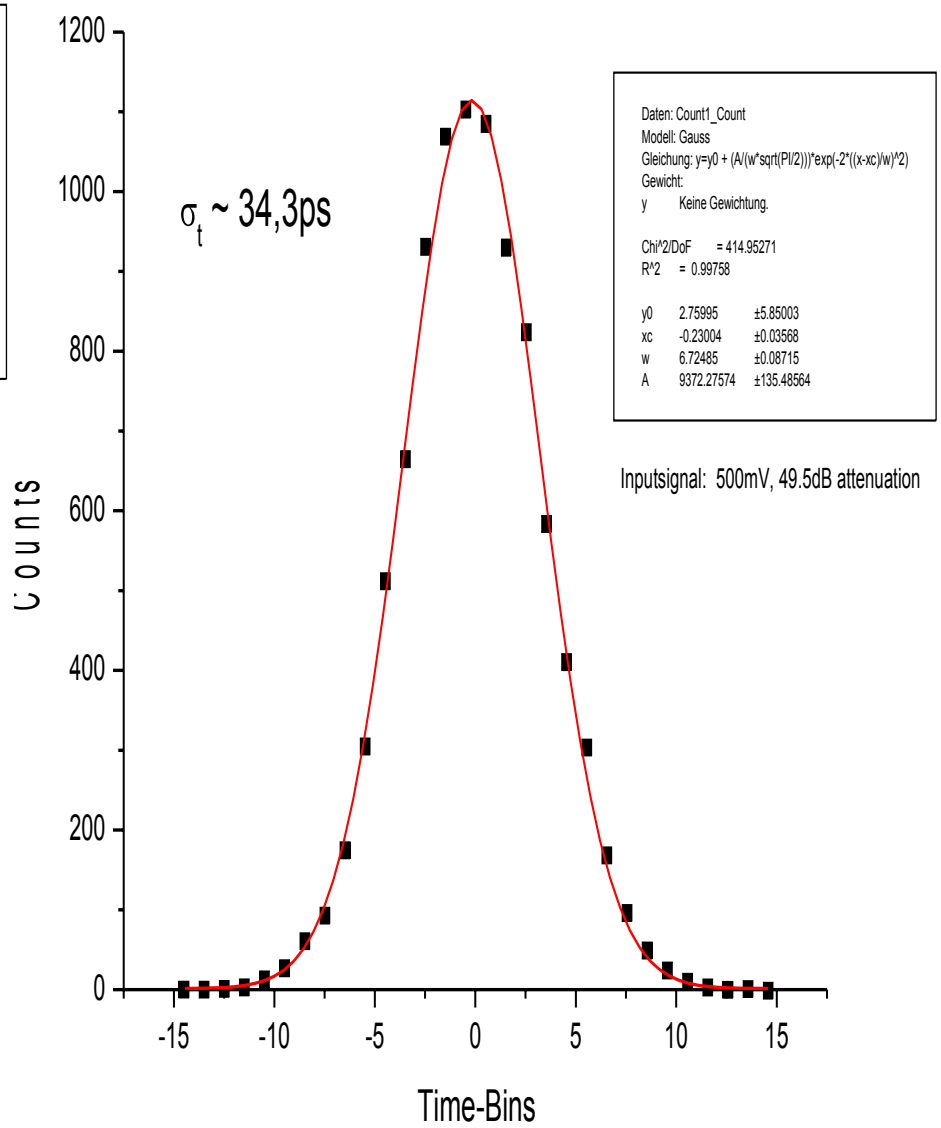
- 16 channels with two NINO2 IC.
- Differential 100 Ohms inputs, differential Time outputs with Time over-Threshold modulation
- OR input and output
- External: Threshold voltage, TEST E/D

Combined Time Resolution of two channels: Input signal is ~1.67mV or ~42fC

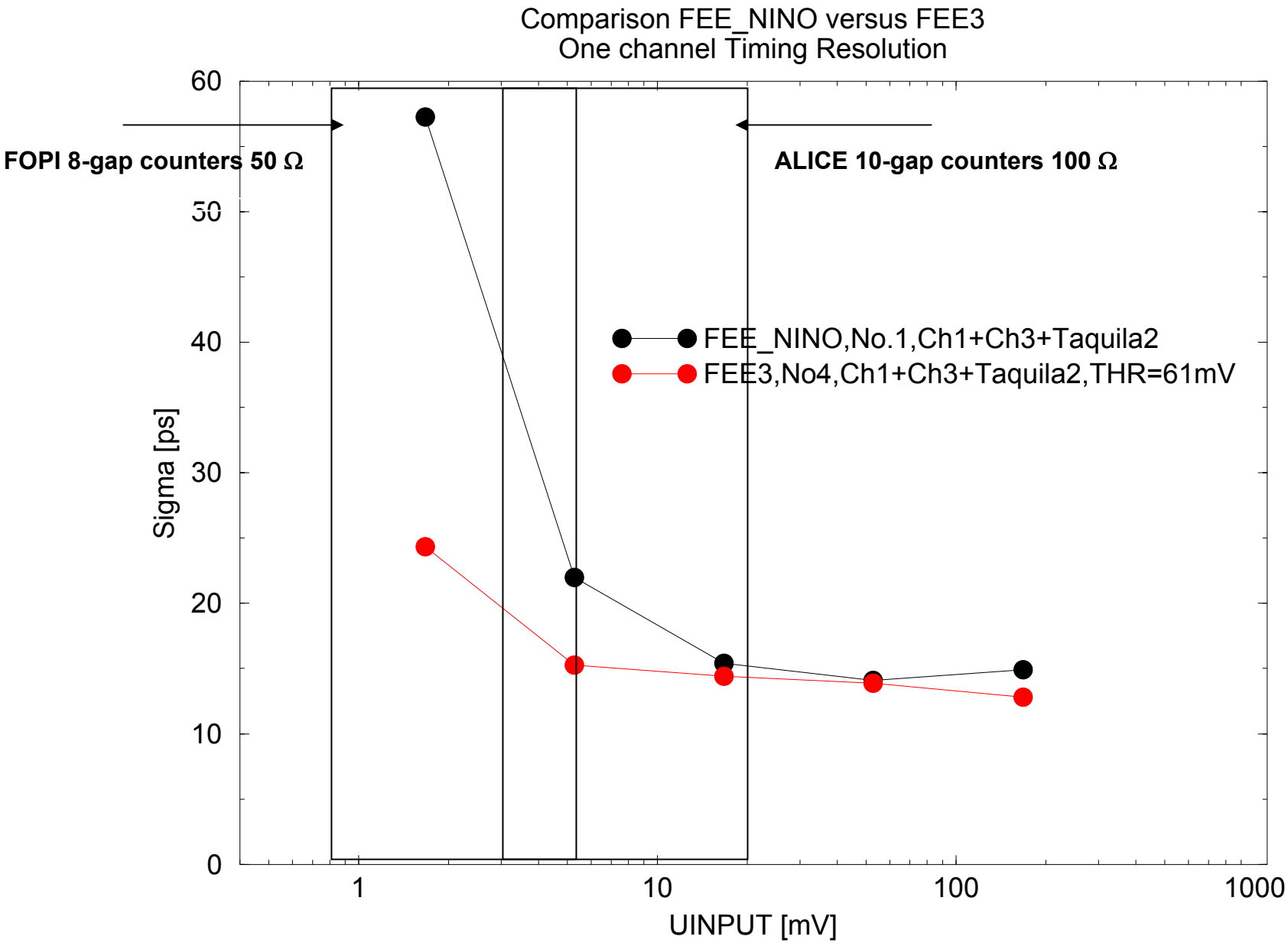
FEE-NINO + Tacquila2



FEE3 + Tacquila2

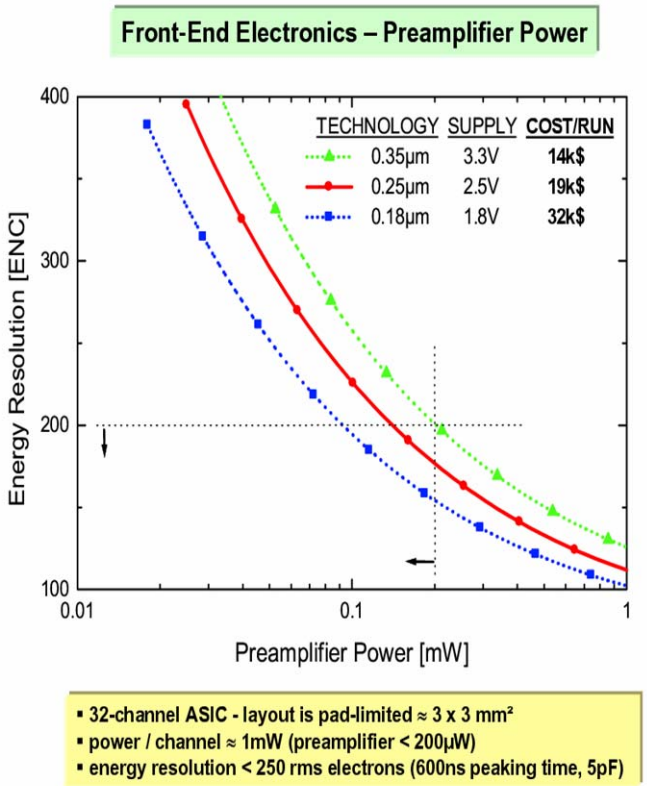


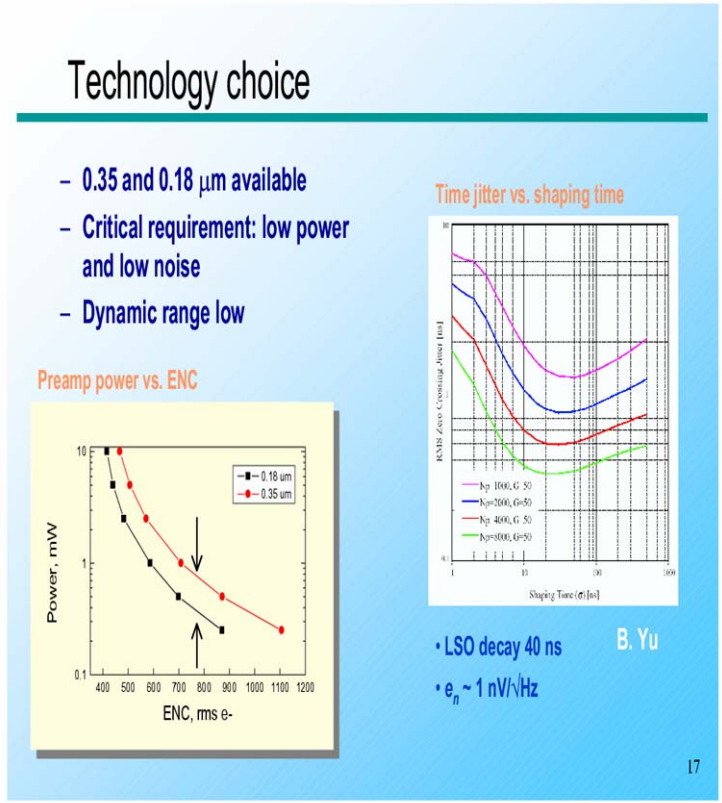
Combined Timing Resolution with TACQUILA 2



About Technology: CMOS : AMS 0.35um or UMC 0.18um?

(AMS – Austria Mikro Systeme International, UMC – United Microelectronics Corp.)





Development of a Front-End ASIC for TEGS TPC
G.De Geronimo, Paul O'Connor, Veljko Radeka, Bo Yu
Vth International Meeting on FEE, 2003

Low noise charge amplifiers in submicron CMOS
P.O'Connor, J.-F.Pratte, G.De Geronimo
Vth International Meeting on FEE, 2003

NINO2 structure

IBM CMOS 0.25 um technology

capacitance (which is the unavoidable stray capacitance associated with the transistor) on the drain; the rise time of this signal is governed by the characteristics of the transistor itself while the fall time is given by the time the capacitance C takes to be recharged (i.e. RC). The input impedance is $(1/g_m)_{M1}$ and therefore the biasing and geometry of M1 is chosen to keep this impedance low to match the transmission line carrying the input signal. The output voltage is defined by the parasitic capacitance C and thus M2 is designed to minimise this capacitance.

A block diagram of the NINO (version 2) is shown in Fig. 3. The input stage is followed by 4 stages of low-gain, high-bandwidth differential amplifier. A slow feedback circuit supplies current to ensure that the input stages remain correctly biased. In addition an offset is added at this point that acts as a threshold adjustment. There is a stretcher just before the LVDS output driver. The pulse width before stretching varies between 2 ns and 7 ns; the HPTDC [3] that will be used in ALICE can only measure both leading and trailing edges of an input pulse for widths greater than 6 ns; thus the pulse stretcher will increase the pulse width by 10 ns.

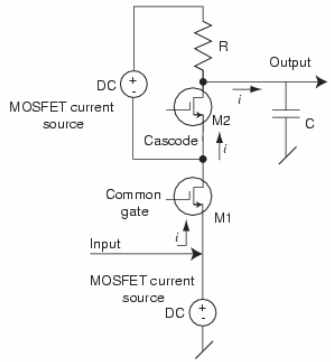


Fig. 2. Schematic input stage of the NINO ASIC.

3. Performance

The performance of the NINO ASIC attached to the MRPC strip was tested at the CERN T10 beam using 6 GeV/c pions. The time t0 of the incoming pion was measured by two scintillator bars read out with 4 Hammamatsu photomultipliers. The time jitter of t0 was 30 ps and was subtracted in quadrature from the measurements of the time resolution of the device under test.

The output of the MAXIM FEA card was ECL pulse for the leading edge and an analogue signal that was measured with a CAMAC ADC (LRS 2249W).

The time of the leading edge has to be corrected for the amplitude of the signal. Thus, this correction was made using the ADC value in the case of the MAXIM FEA and using the time width for the NINO FEA. The time width of the output pulse from the NINO ASIC varies rapidly for

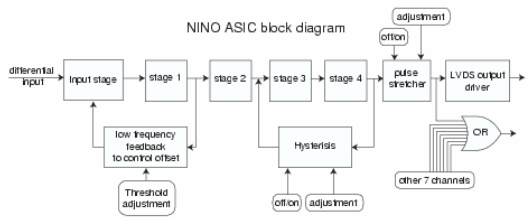
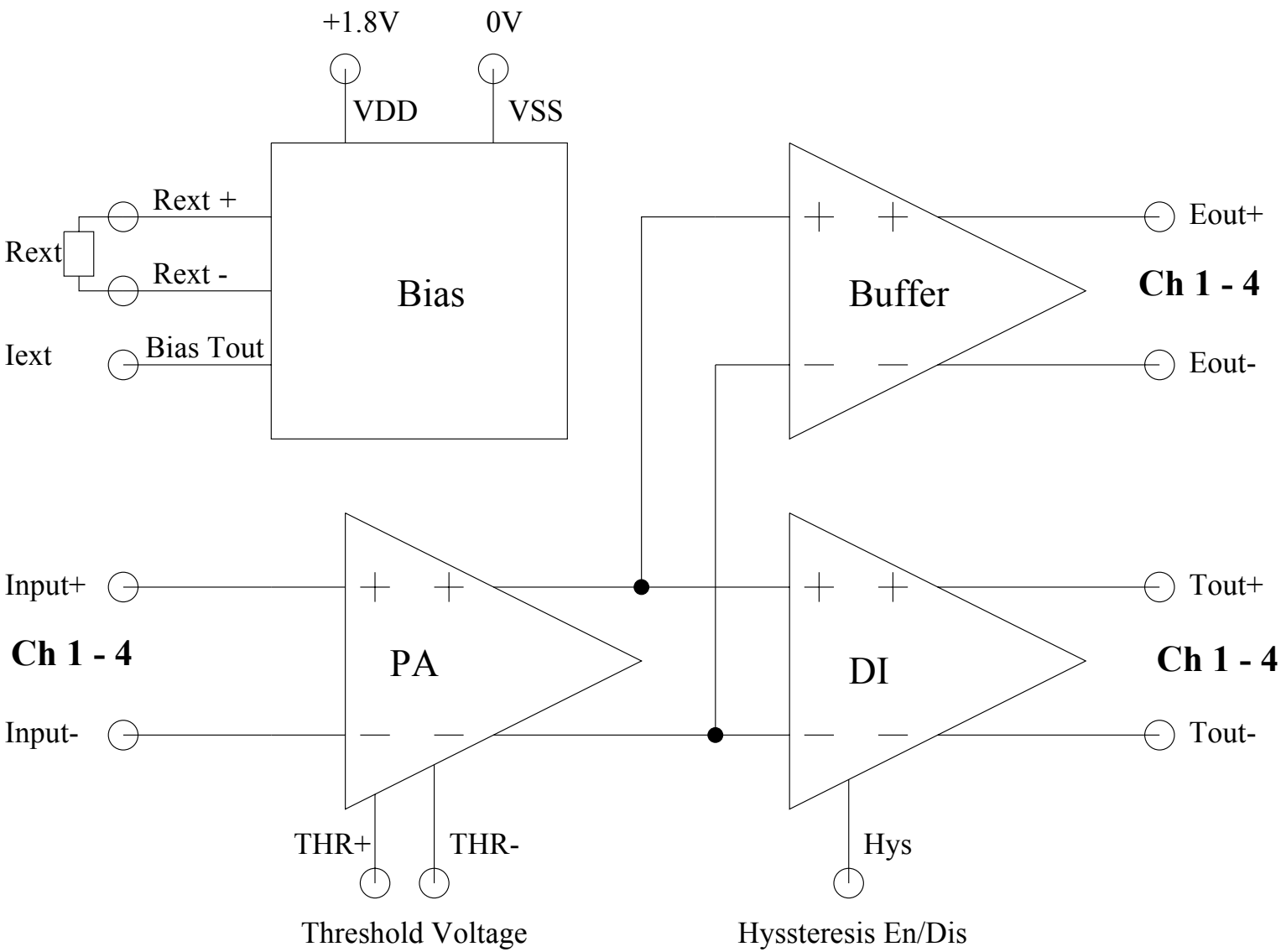


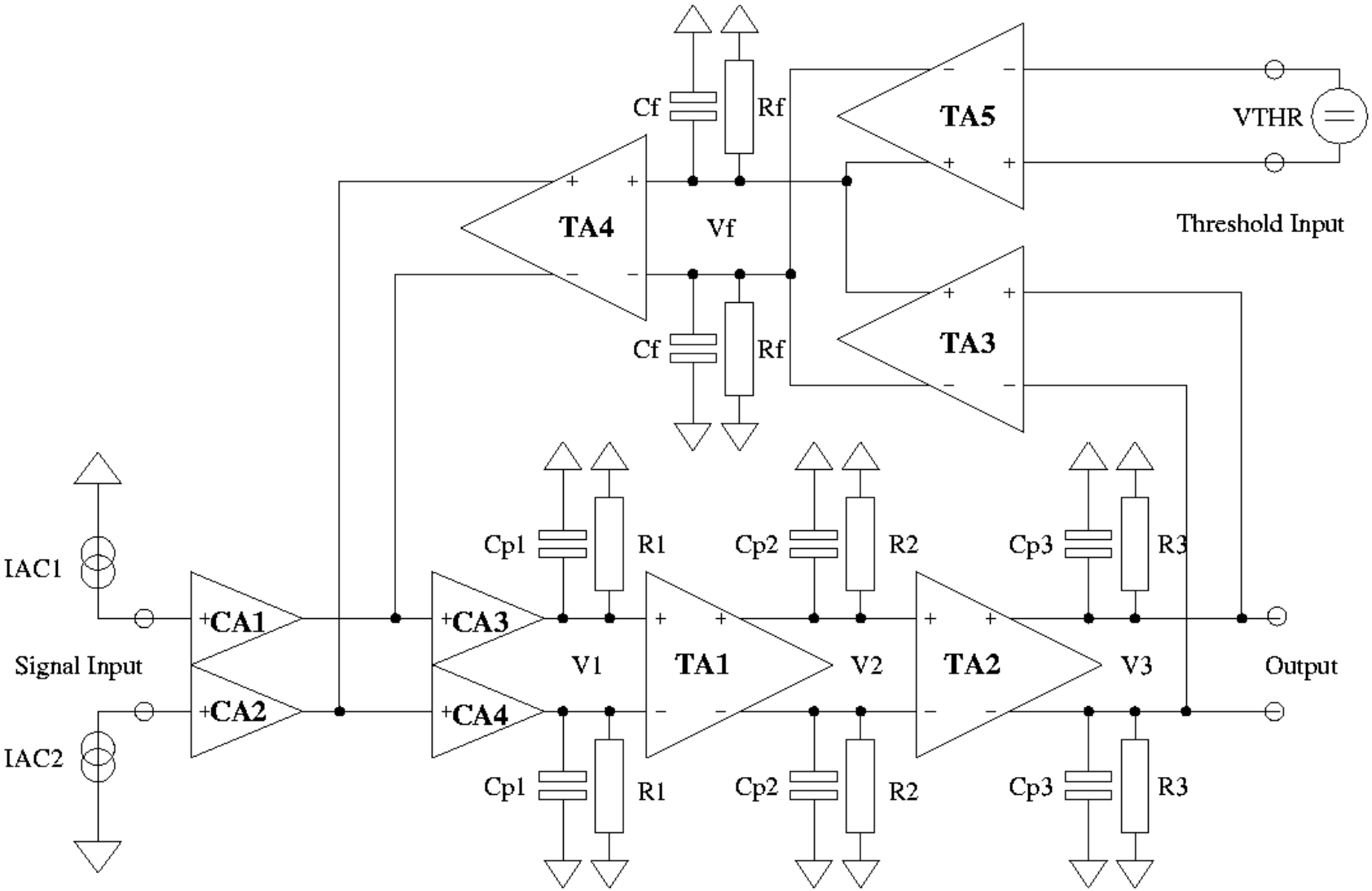
Fig. 3. Block diagram of the NINO ASIC.

F.Anghenolfi and al, NINO: an ultra-fast and low-power front-end amplifier/discriminator ASIC designed for the multigap resistive plate chamber, Nuclear Instruments and Methods in Physics Research A 533 (2004) 183-187

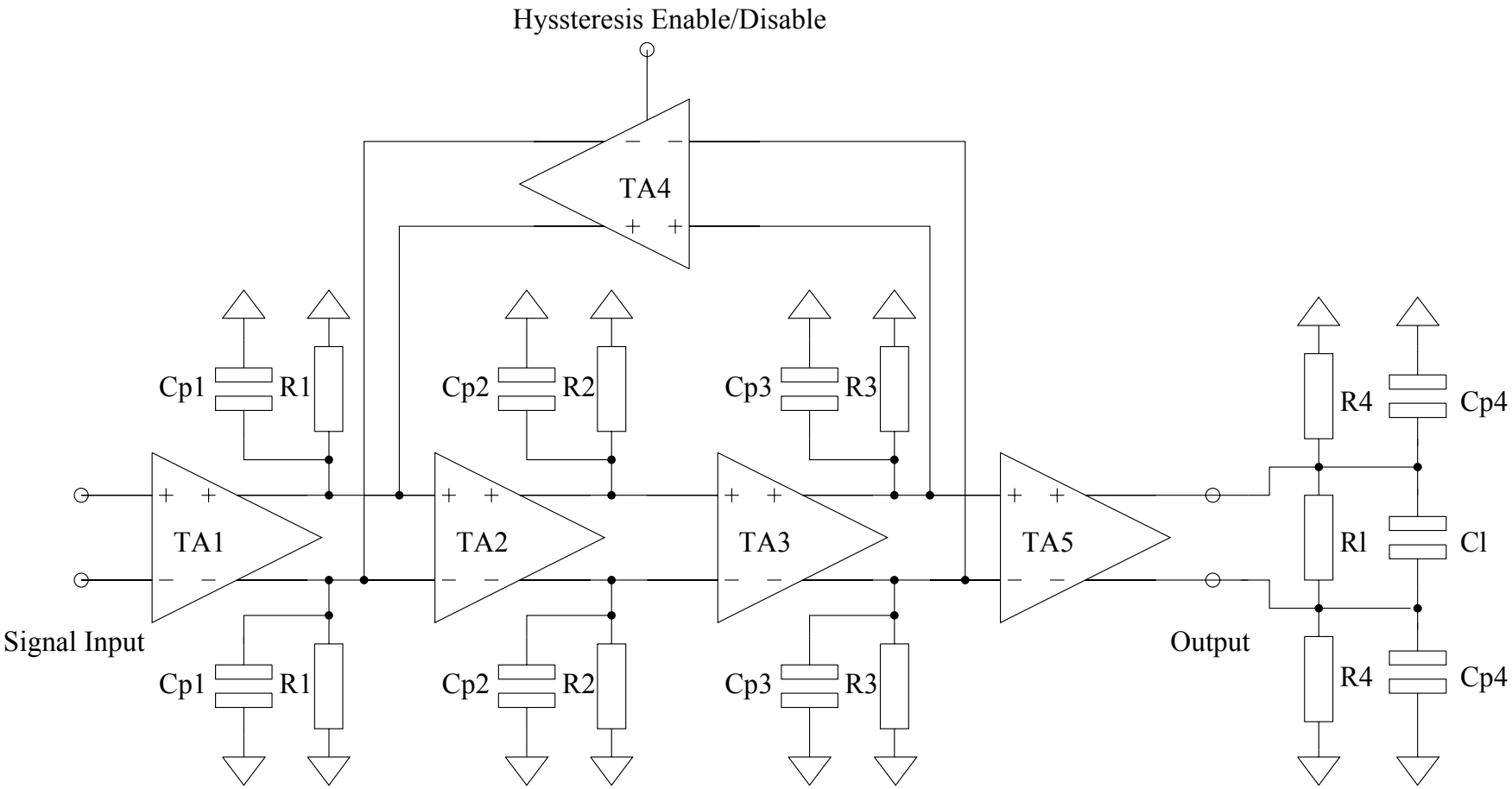
PADI block diagram



Preamplifier: AC equivalent diagram



Discriminator: AC equivalent diagram



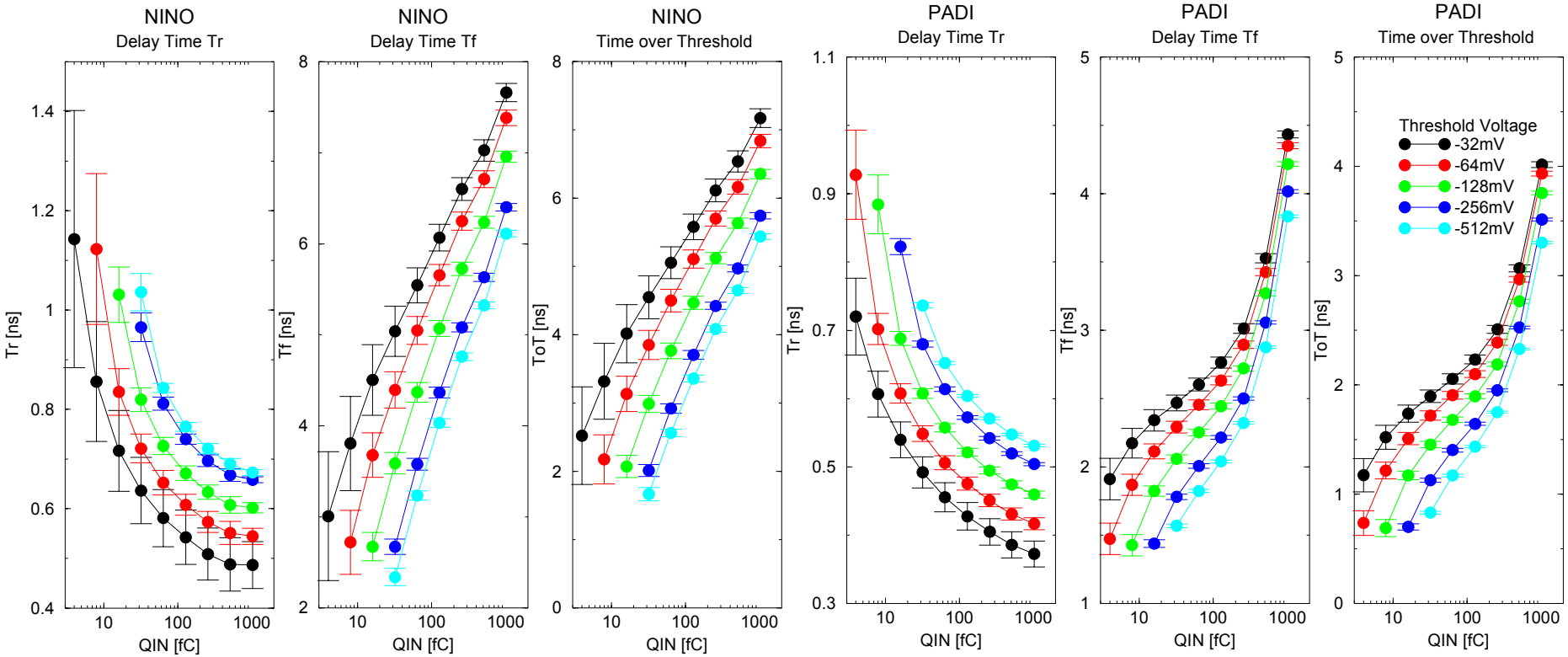
AC simulations

	PADI sch.		PADI sch. with Cp.layout		NINO1 sch.	
	Gain [dB]	BW [MHz]	Gain [dB]	BW [MHz]	Gain [dB]	BW [MHz]
Preamplifier						
Low pass corner	27	12	27	12	31.6	5.5
PA Out	48	420	48	360	51	120
Buffer						
Eout	-1.1	10000	-1.1	8800	-	-
Discriminator						
TOut, Hys=off	48.3	280	48.3	260	47	180

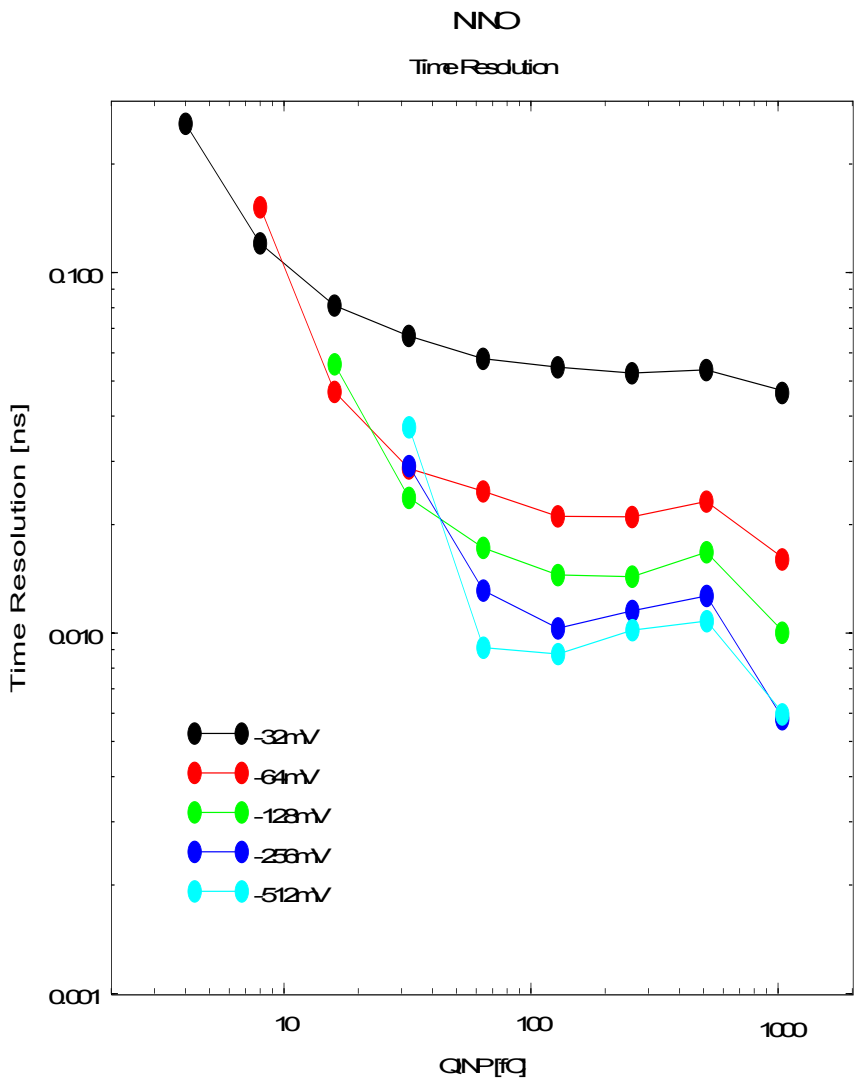
Noise on PADI Preamplifier:		**sch.**		**sch.whith Cp. layout**	
Simulation BW	[MHz]	500	1000	500	1000
Noise PA Out	[mV RMS]	4.52	5.17	4.35	4.84

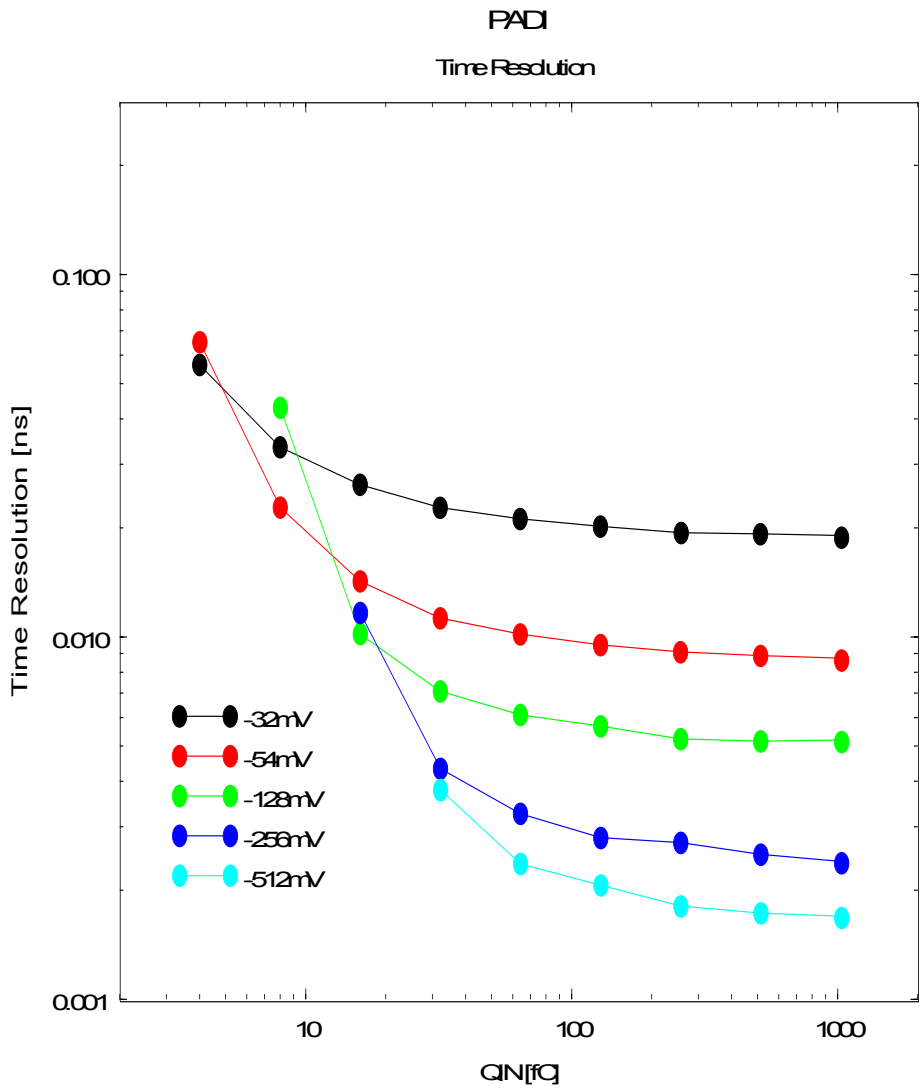
Noise on NINO1 Preamplifier sch.			
Simulation BW	[MHz]	500	1000
Noise PA Out	[mV RMS]	3.83	3.91

Comparison on Delay Times
NINO versus PADI

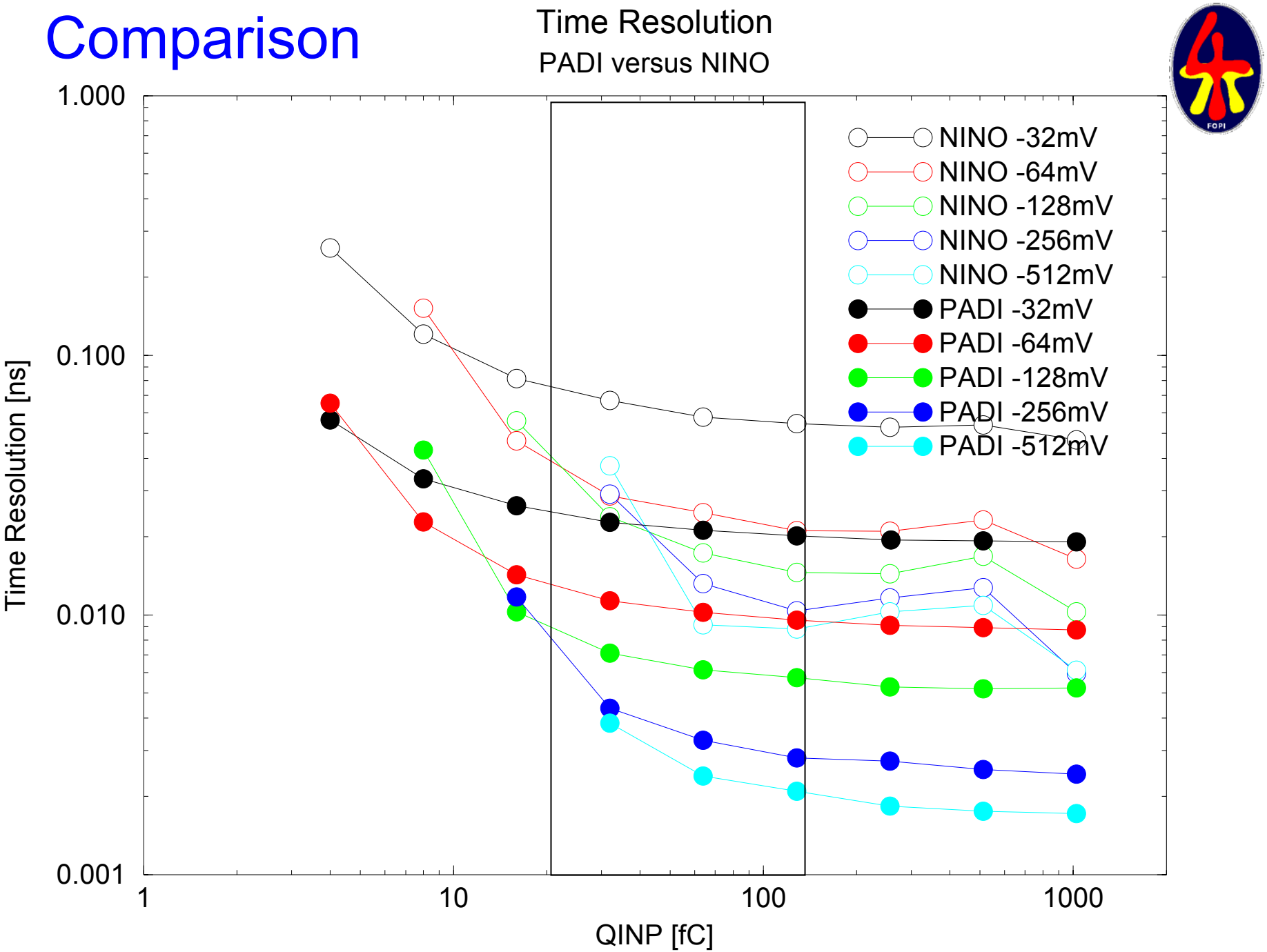


Comparison on Time Resolution: NINO versus PADI

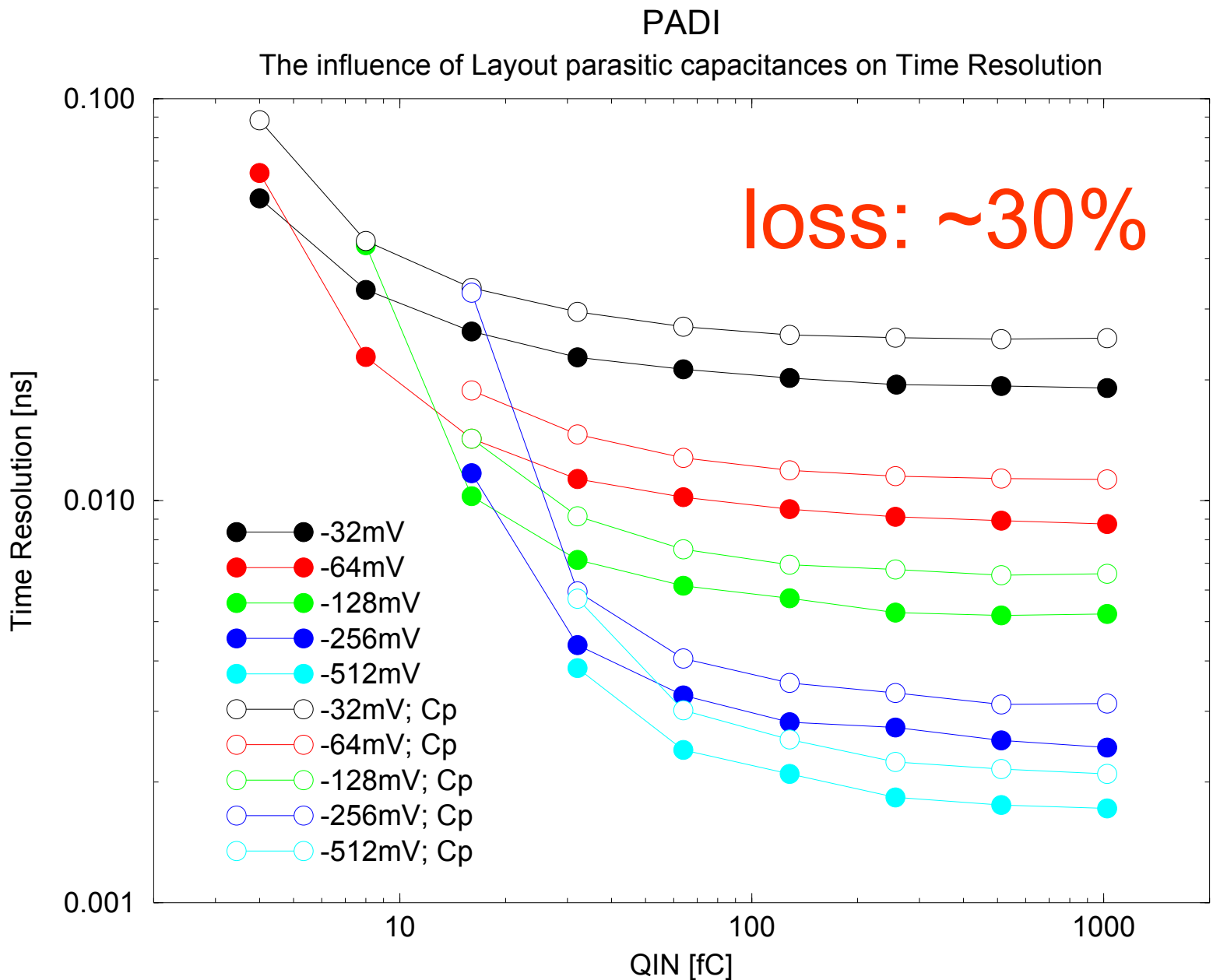




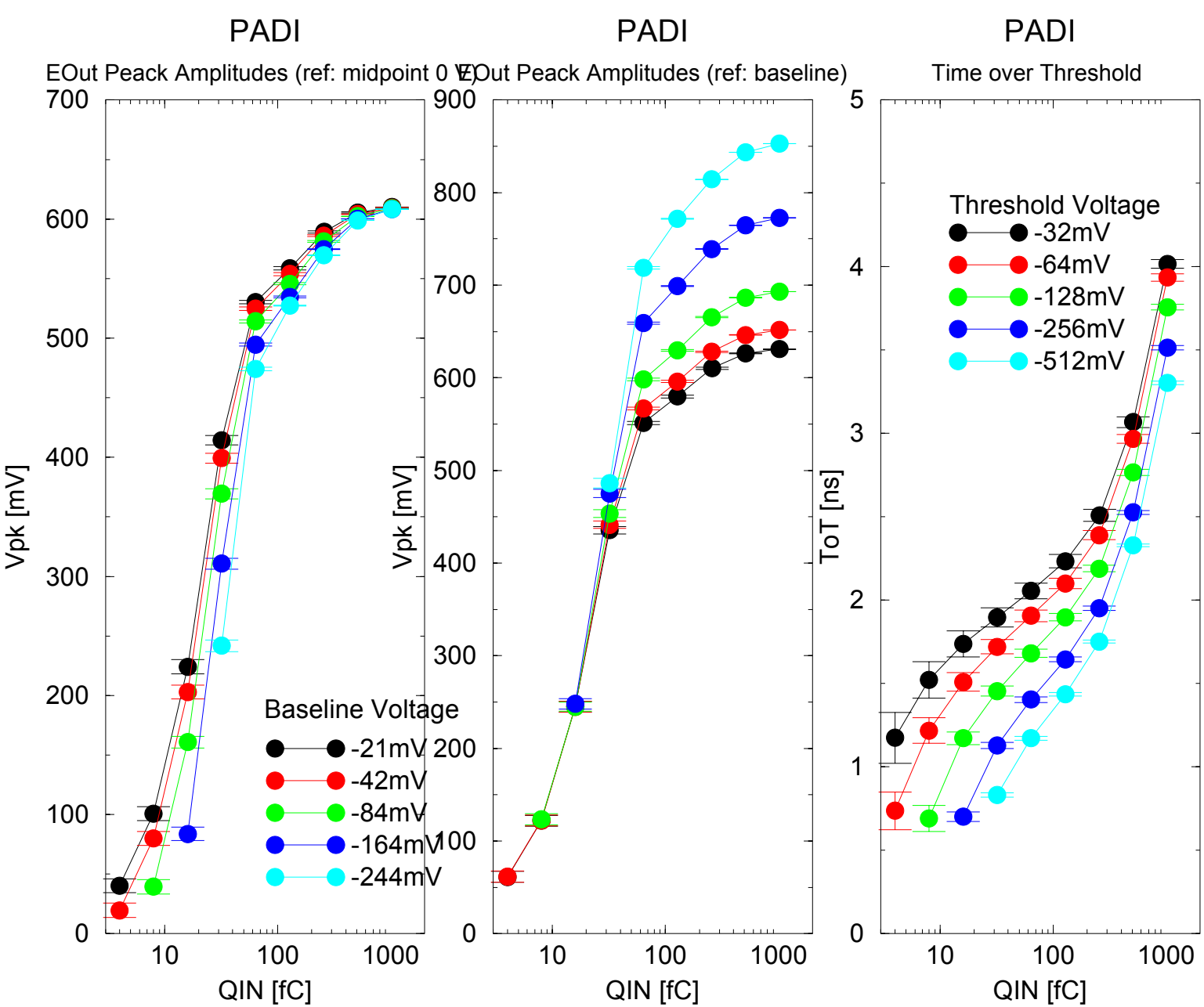
Comparison


Time Resolution
PADI versus NINO
1.000
0.100
0.010
0.001
Time Resolution [ns]
1
10
100
1000
QINP [fC]
NINO -32mV
NINO -64mV
NINO -128mV
NINO -256mV
NINO -512mV
PADI -32mV
PADI -64mV
PADI -128mV
PADI -256mV
PADI -512mV

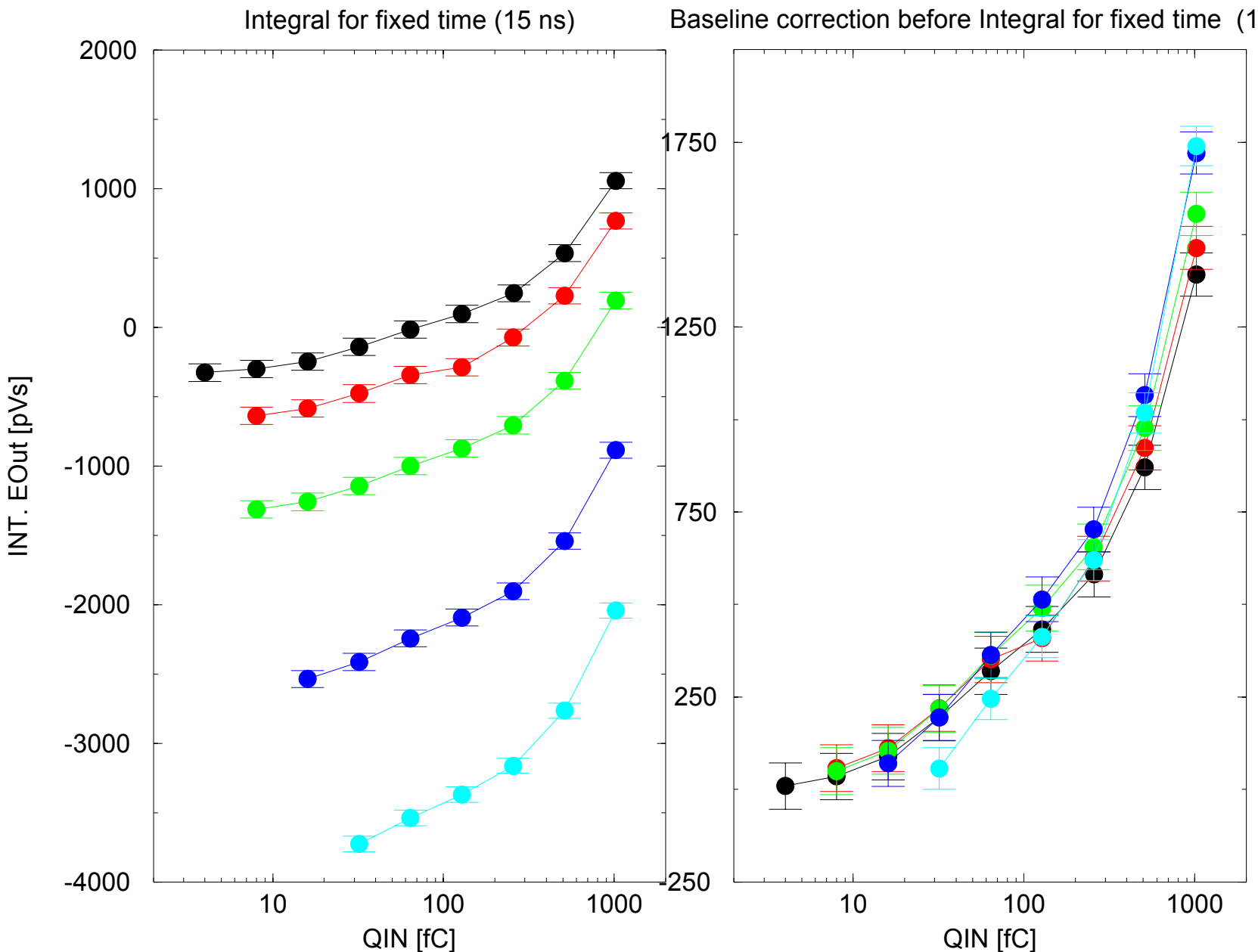
PADI The Layout parasitic capacitance increase the Time Resolution

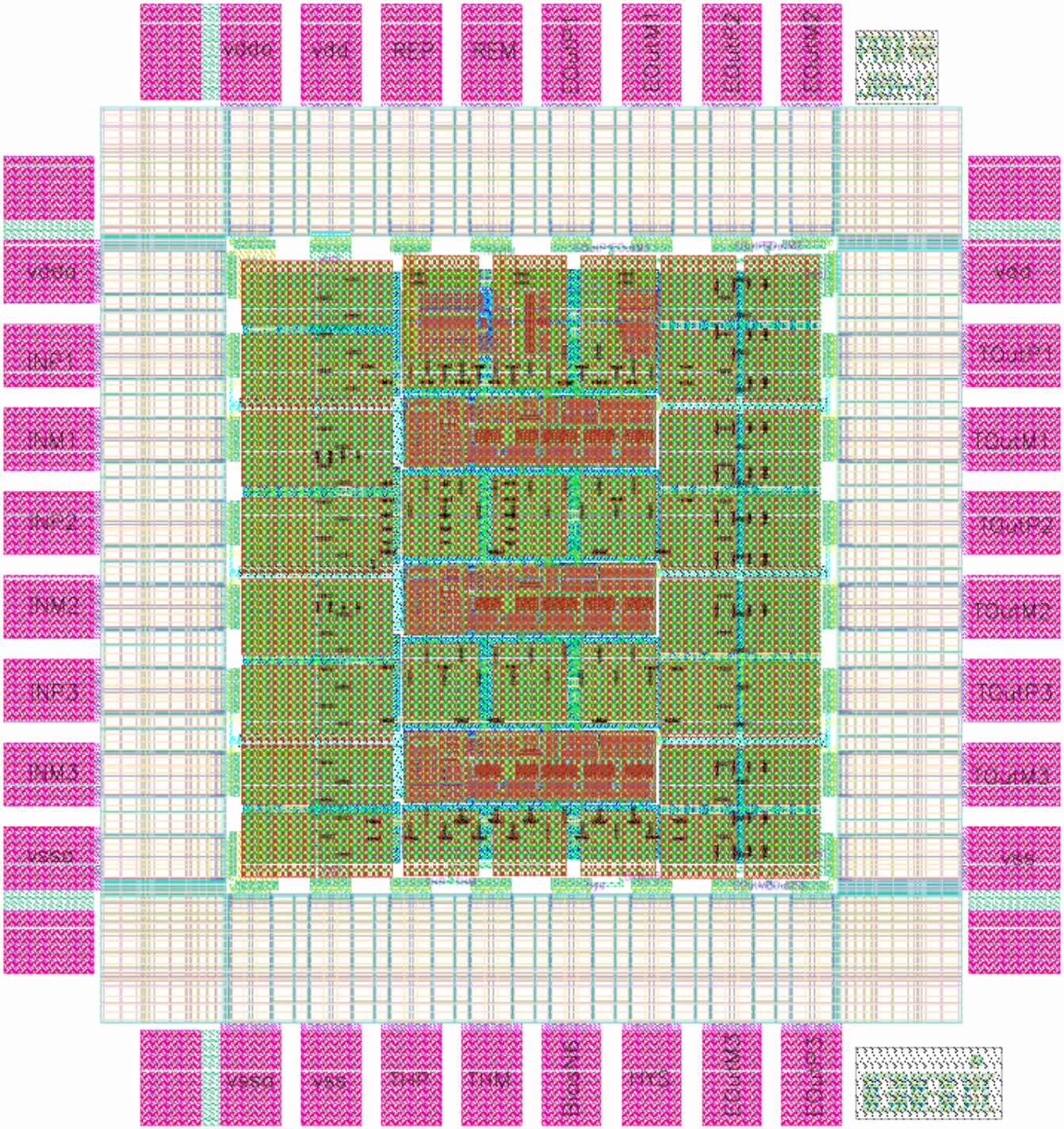


WALK Correction: Time over Threshold or Q measurement?



WALK Correction: .... or Integrated Q measurement?





PADI

!NEW ASIC!

the prototype has only 3 channels Preamplifier & Discriminator in

0.18µm CMOS technology

1.5x1.5mm2

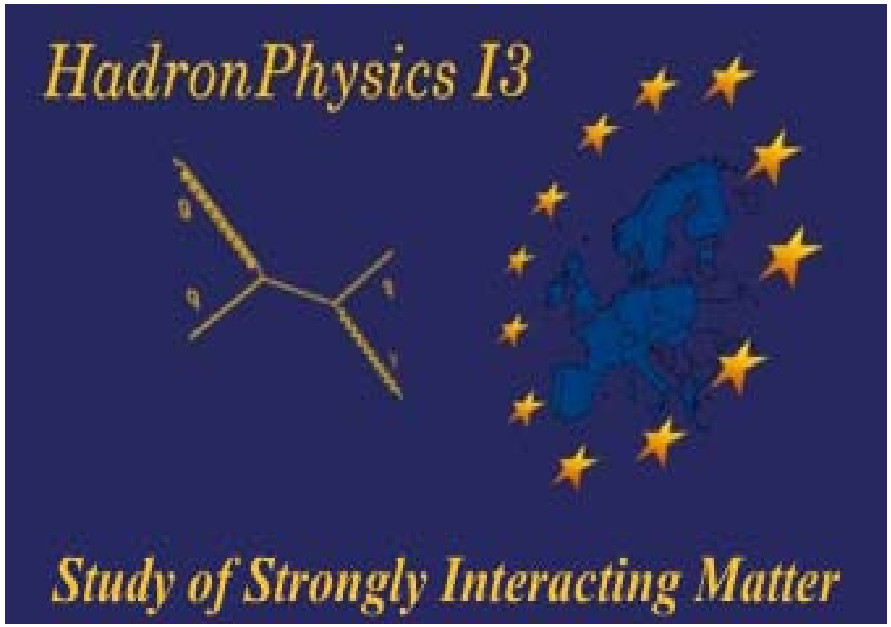
Summary

- FEE3 vs FEE-NINO

  Due to the full differential structure, FEE-NINO has a lower sensitivity to pick-up of parasitic signals. To use all benefits of this design, the detector must be differential too.

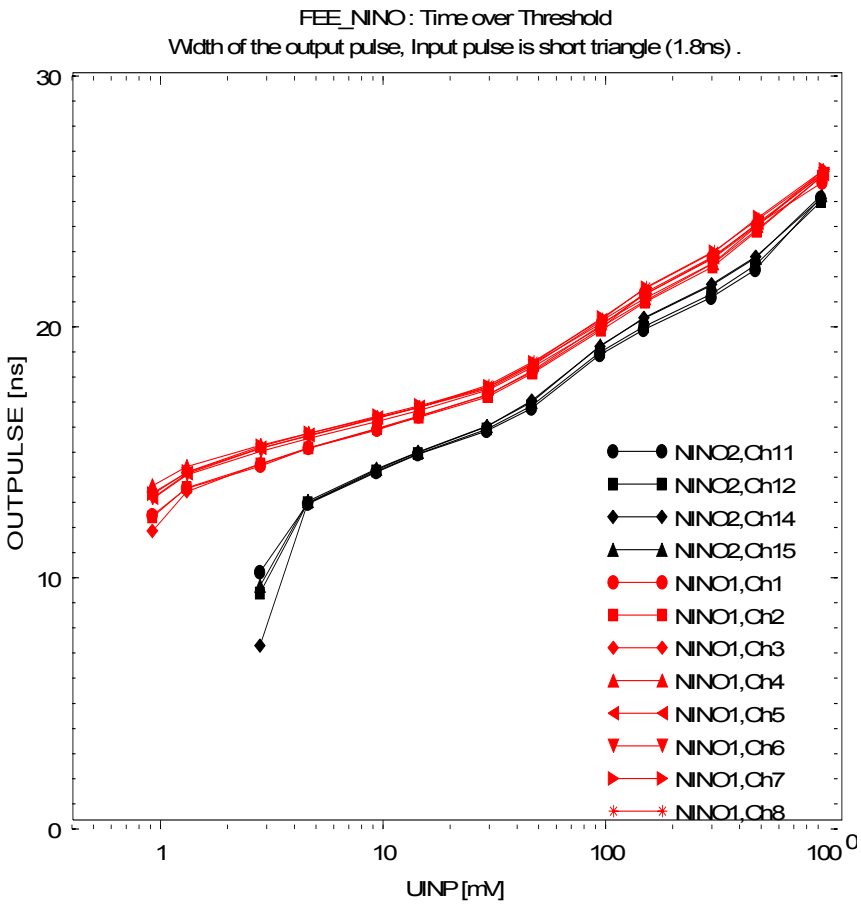
Outlook

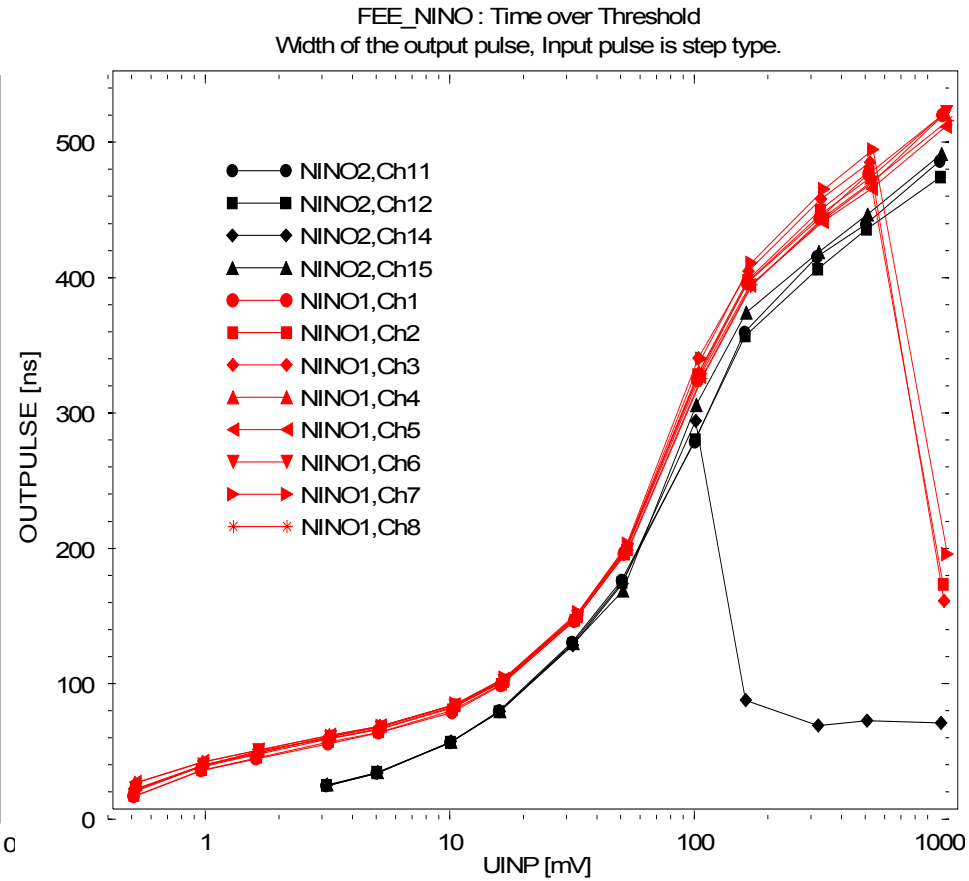
- We wait for first PADI chips for tests.
- The increase of PADI preamp/discriminator actual bandwidth is a hard task, but we will try to evaluate the limit of the used architecture.
- We will investigate the possibility to change the biasing type, from voltage to current, to decrease the crosstalk inside the PADI chip.



We acknowledge the support of the European Community-Research Infrastructure Activity under the FP6 "Structuring the European Research Area" programme (HadronPhysics, contract number RII3-CT-2004-506078).

Time over Threshold tests for FEE-NINO





Time Resolution measured with TDS 7104 Oscilloscope 1.3 GHz