Electronic Systems for the CBM Experiment at FAIR

Developments at GSI

Holger Flemming, EE
Overview

• DLL Testchip, Designed by Harald Deppe
  • Results of DLL Testchip
• First TAC Testchip in 180 nm CMOS technology
  • Time to Amplitude Converter
  • Chip Design
    • Simulation
    • Layout
    • Test

• Next Steps
• Conclusion
DLL based TDC Core for Time of Flight Measurements

Chain of N identical delay elements with adjustable delay, phase detector and charge pump.

Advantage:
Self Calibration to compensate temperature and process variations.

Intrinsic resolution of a DLL is determined by the delay of a basic cell:

\[ T_{\text{Bin}} = \frac{T_{\text{ref}}}{N} \]

HERE: 128Bins => 97.65ps @ 80MHz.
Main Results of DLL Testchip

- Power consumption:
  - VDDIO: 5,5 mA @ 3,3 V ⇒ 18,5 mW
  - VDDA: 6,5 mA @ 1,8 V ⇒ 11,7 mW
  - VDDD: 1,5 mA @ 1,8 V ⇒ 2,7 mW

- Clock jitter at LastDummyOut: 6,8 ps rms

- Lock range: 65 to 95 MHz

- Time resolution:
  31,8 ps ± 0,17 ps

- DNL: +0,37 / -0,81 LSB
- INL: +0,66 / -1,07 LSB
Next Step for DLL Evaluation

- 4
- 4
- =
- C
TDC Core with a Time to Amplitude Converter (TAC)

- Digital delay chain
- Distributed RC-Network
- Voltage on $C_{out}$ increases linear with time

Benefits
- Time resolution not limited by delay of a digital element
- Time resolution below 10 ps possible
- Zero power consumption in standby mode

Drawbacks
- Calibration necessary
- Deadtime during ramping and readout
First GSI TAC Implementation

TAC based TDC already successfully implemented

- TAC-ASIC by GSI and FhG IMS in 0.8µm CMOS
- Used in FOPI RPC Readout
- Time resolution better than 10 ps
First TAC Testchip in 180 nm

- 2 TAC TDC Cores
- SC attenuator to avoid rail to rail signals
- Common clock and analog output
- LVDS inputs
- Some more teststructures
Simulation of First Testchip

Time to Amplitude Characteristics

Output Voltage [mV] vs. Start Time [ns]

Data from "tac_kenn5.dat"

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3rd NoRDHia Workshop
Layout of Testchip

- Delay Element
- Tri State Driver
- Power Bars

TAC Core with 48 Elements
Layout of Testchip

SC Attenuator
Layout of Testchip

First TAC Testchip in 180 nm

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Chip submitted in april 2006

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Status of Chip Tests

• First TAC Testchips back at GSI
• Layout of Test-PCB finished
• But:  Some Trouble with first PCB delivery
  • PCBs not bondable
• Second charge of Test-PCBs better
• Just now: Bonded Chips on Test-PCBs
Next Steps

• Measurement of Chip Performance
  • Time Resolution
  • Nonlinearity
  • Crosstalk
  • Sensitivity on Noise from digital Logic (Substrate Coupling)
Concept for Complete TAC based TDC

- Time over Threshold measurement for signal amplitude determination
- Integrating TAC and ADC for converting time to digital
- Timestamp unit for Eventmarking
- Integrated Interface to DAQ
Conclusion

- GSI EE Department is strongly involved in high resolution time measurement for CBM
- Two concepts under evaluation
- First results of DLL are very promising
- First results of TAC expected soon