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#### Using NINO, an ultra-fast, low-power, front-end amplifier discriminator for Diamond detectors. TOF ALICE DETECTOR (LHC CERN)

•The TOF detector using MRPC strips. The area of the detector is ~160 square meters.

•The system has total number of read-out channels (pads) equal to ~160.000.

TOF



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#### Input stage

- Common gate circuit with very high bandwidth @<0.5ns peaking time
- The input charge is flowing through the output load (RL\*CL=1ns), while the input impedance is low
- Input impedance (1/gmsb) is tuned to match the impedance of detector signal transmission lines
- No signal feedback, fully differential DC coupled structure is ideal for high data rates and large signals dynamic range.



Input stage (half of fully differential circuit)



#### Preamplifier schematic

- Fully differential structure from input to output
- Gain of PA stage is 30,
- Gain is obtained by 4 consecutive stages as .
   High bandwidth low gain stages (G=6, BW=500Mhz)
- Last stage is a open-drain differential pair to provide LVDS like outputs

#### NINO channel structure



- Minimum threshold at 5–10fC.
- < 3000 el. Noise @ 6pF Cdet
- Tunable differential input impedance on the range (40– 100) Ohm.
- < 9 ps rms front edge time jitter
- Hysteresis value can adjust up to 12%
- Pulse width variable from 0.5ns up to 6ns vs. input charge.



Noise vs. Cin for liner range

< 3000 el. Noise @ 6pF Cdet,
Rext is 25 Ohm



equivalent input charge is 30fC,
Rext is 25 Ohm,
additional stretch time value is 12ns

Limiting of NINO ASIC for diamond applications



- Input DC offset voltage (equivalent of amplification factor) is a limit of minimum detectable charge over 5-10 fC,
- Input noise level (< 3k el. @ 6pF Cdet) is provide of levels discrimination from ions beams counters,
- Dependence of output pulse width from detectable charge is limiting of maximum data rate over 10e9 particle/s

### Proposals for using NINO ASIC for diamond applications

Increasing of maximum data rate:

- Using NINO ASIC on standard mode: Qmin = 5-10 fC, output pulse width range from 0.5ns up to 6ns, max. data rate over 100 - 400 MHz,
- Using NINO ASIC on inverting mode for realizing maximum data rate 400 1200MHz with (0.5 –1) ns normalization output pulse width,
- Using constant fraction method for normalization input charges by value (on inverting NINO mode) for providing maximum data rate up to 1200 GHz.
- Using ultra fast 1.2 GHz prescalers with divide ratio 10 are connecting to itch NINO outputs directly for realizing full data rate and reducing limitation for transport cable.

### Proposals for using NINO ASIC for diamond applications

#### Increasing of input sensitivity:

- Using NINO ASIC on standard mode: Qmin = 5-10 fC,
- Using additional external ultra fast @ low noise preamplifier (such as ATF-54143, Ajilent HEMT or GALI-S66) with amplification factor Av > 10 and < 1500 el@Cdet = 0 pF noise, > 1 GHz bandwidth should provide 1fC of estimation minimum detectable charge.
- Note: For saving differential front end structure should use two preamplifiers per NINO channel.







The NINO ASIC bonded to the PCB

- IBM 0.25 um Si CMOS technology
- 8 channels, 2x4 mm<sup>2</sup> chip
- Channel power is 27mW
- +2.5V supply voltage only
- Delay time 1ns
- Easy operating and controlling



The NINOTAPP final package

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