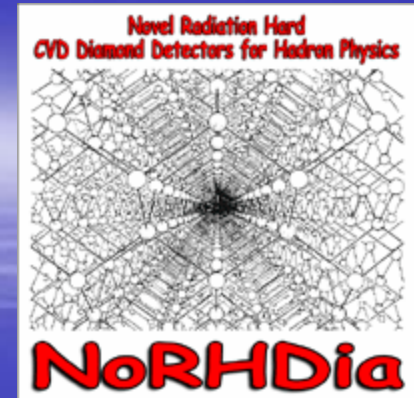




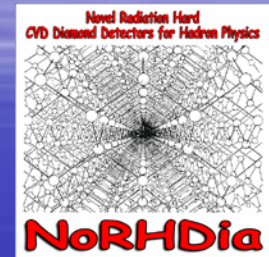
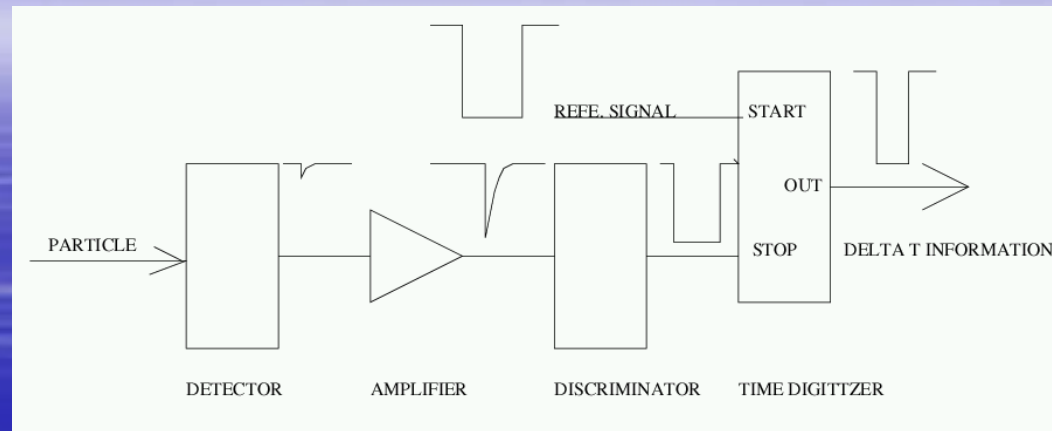
DBA based multi-channel devices

Mircea Ciobanu

NoRDHia Meeting 5-6 July
2004

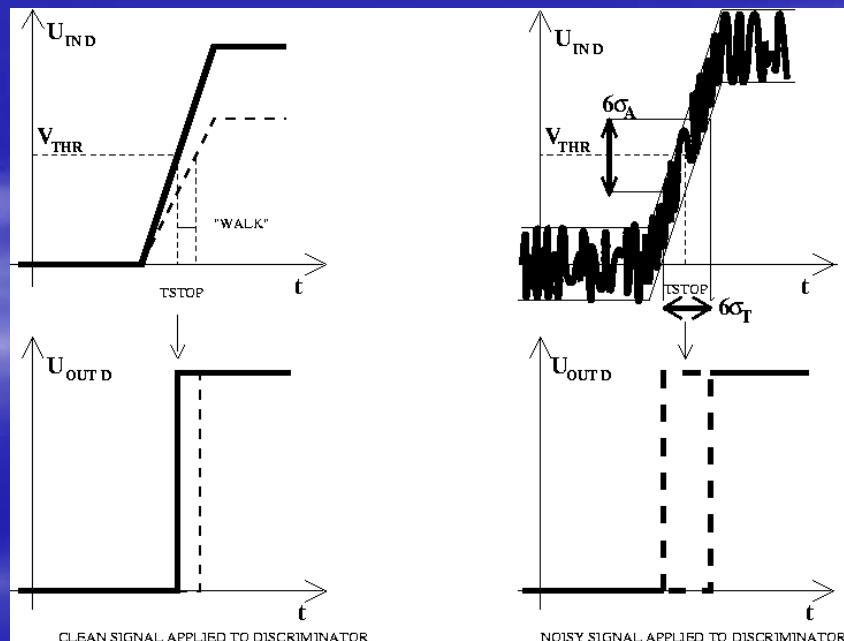
GSI-Darmstadt

Basic components of a Timing Channel



Typical Errors

" WALK "



$$\sigma_t = \frac{\sigma_n}{\left. \frac{dV}{dt} \right|_{V_{THR}}}$$

$$\sigma_t = \frac{\sigma_n}{\left. \frac{dV}{dt} \right|_{V_{THR}}} + \delta t$$

" JITTER "

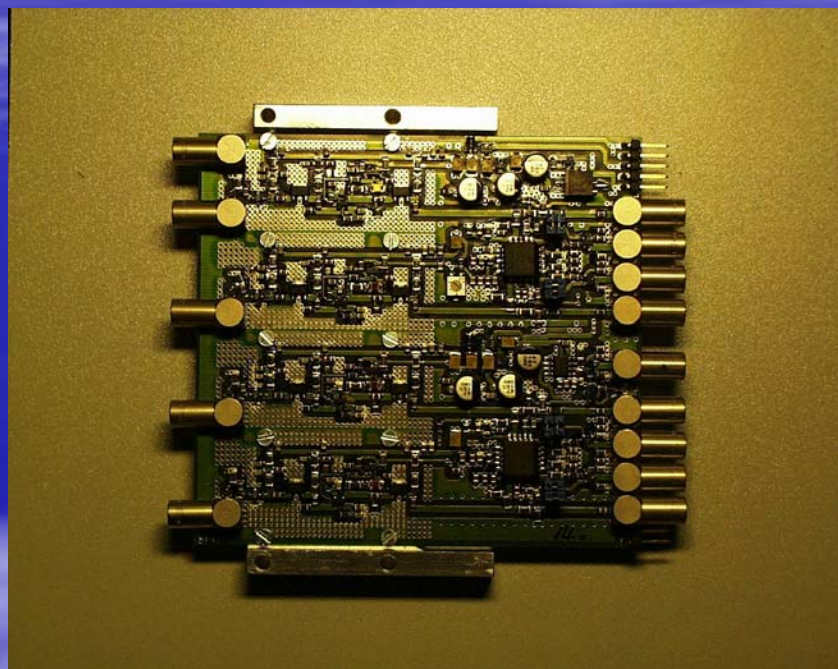
$$\sigma_t \approx \frac{\sqrt{t_c}}{V_o} \sqrt{\frac{t_c}{t_{ra}} + \frac{t_{ra}}{t_c}}$$

has a minimum for

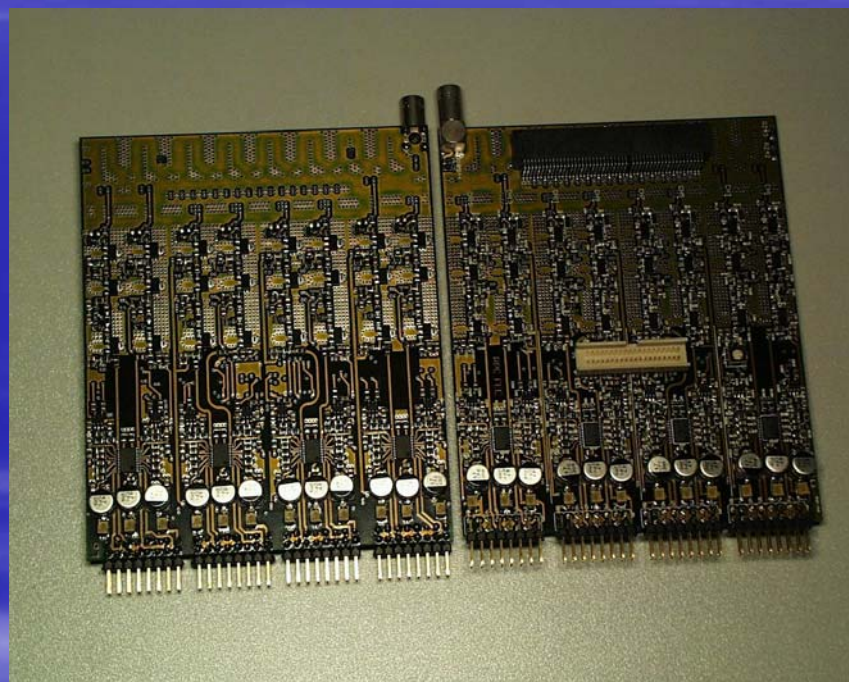
$$t_c = t_{ra}$$



RPC-FEE1 and FEE2

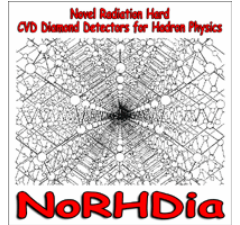


FEE1

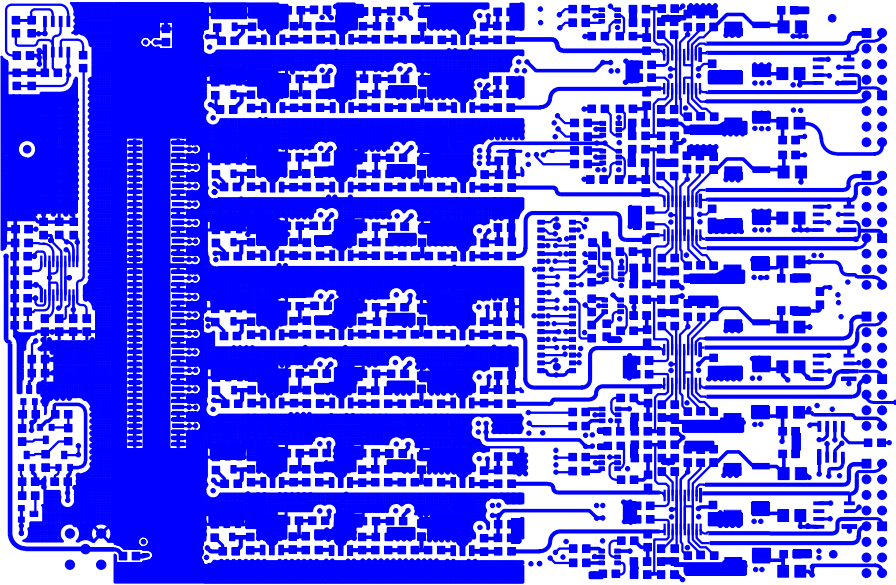


FEE2

FEE2



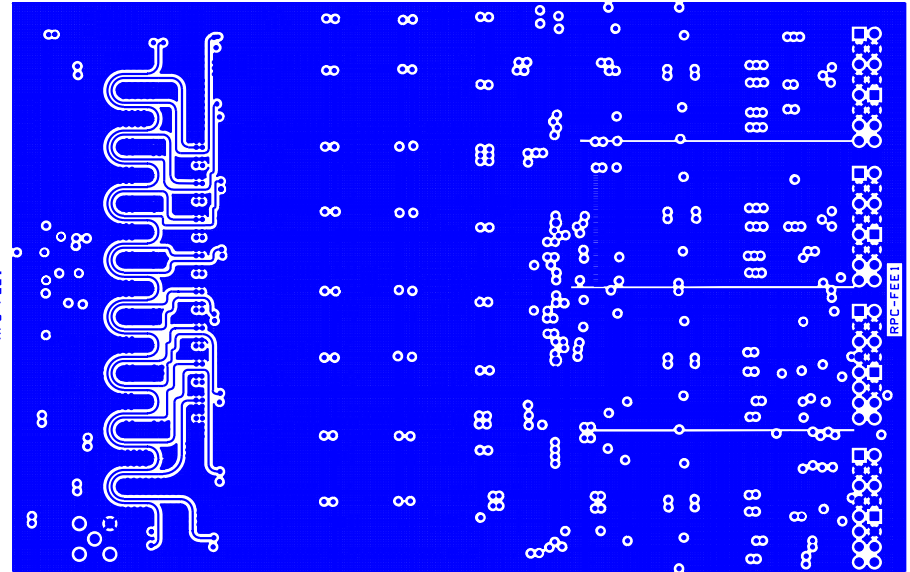
PCB TOP-LAYER



Jobname	Date	Designer	Layouter
RPC-FEE1	1.9.2003	Ciobanu@gsi.de	Ciobanu@gsi.de

[Layer Nickname](#) [Top](#)

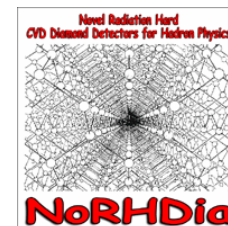
PCB INNER1-LAYER



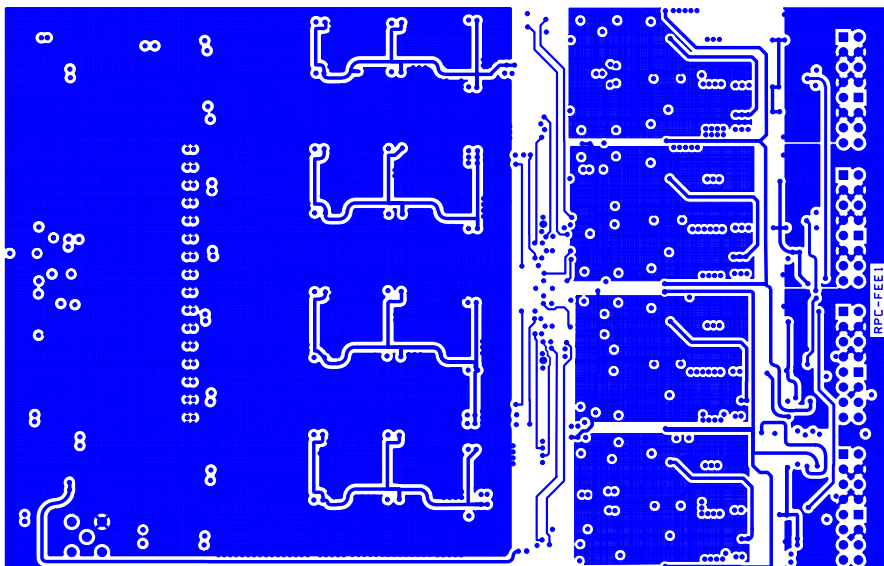
Jobname	Date	Designer	Layouter
RPC-FEE1	1.9.2003	Ciobanu@gsi.de	Ciobanu@gsi.de

IN
LAWYER NICHOLSON

FEE2



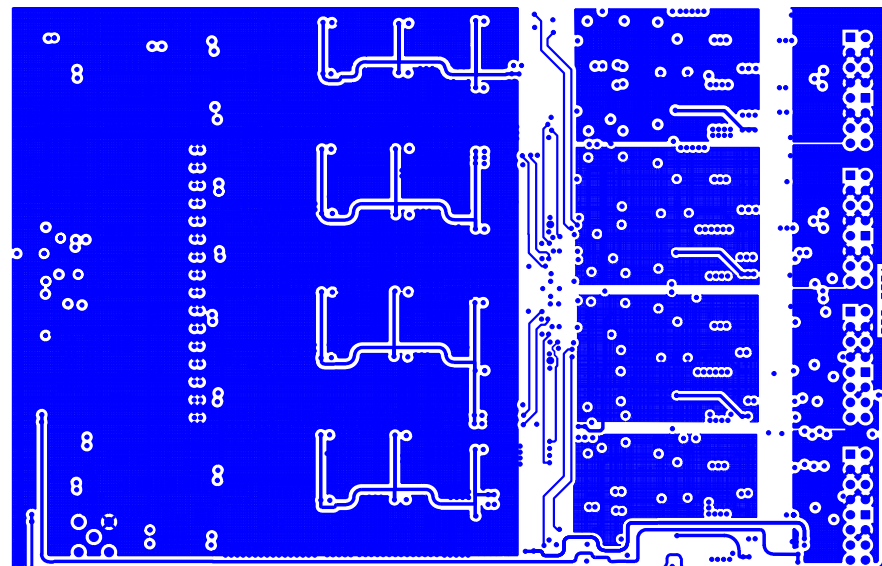
PCB INNER2-LAYER



Jobname Date Designer Layouter
RPC-FEE1 1.9.2003 Ciobanu@gsi.de Ciobanu@gsi.de

Layer Nickname
In2

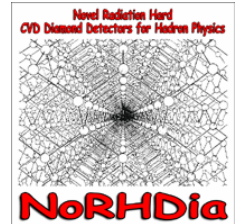
PCB INNER3-LAYER



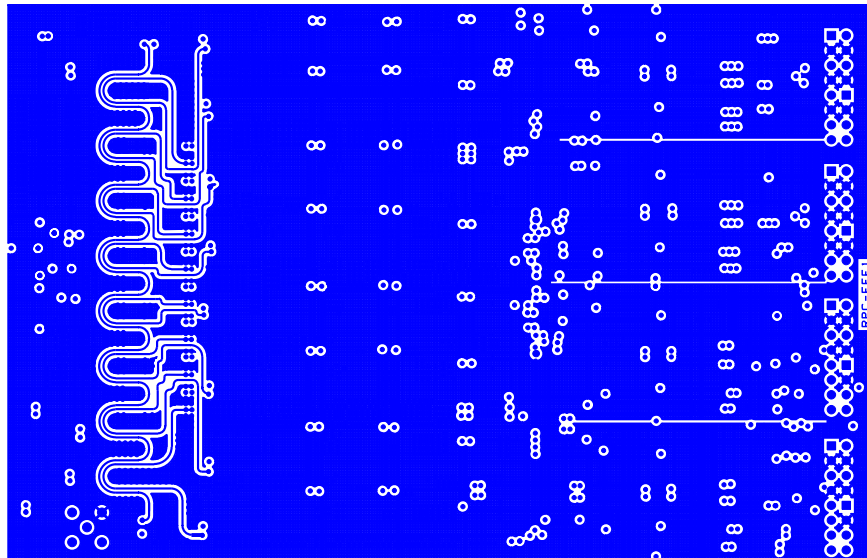
Jobname Date Designer Layouter
RPC-FEE1 1.9.2003 Ciobanu@gsi.de Ciobanu@gsi.de

Layer Nickname
In3

FEE2



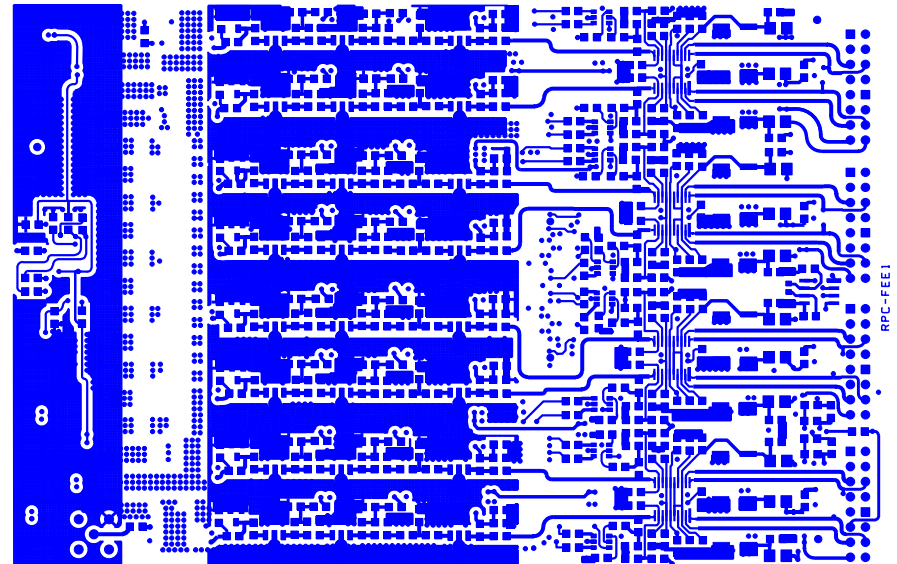
PCB INNER4-LAYER



Jobname Date Designer Layouter
RPC-FEE1 1.9.2003 Ciobanu@gsi.de Ciobanu@gsi.de

Layer
In4

PCB BOTTOM-LAYER



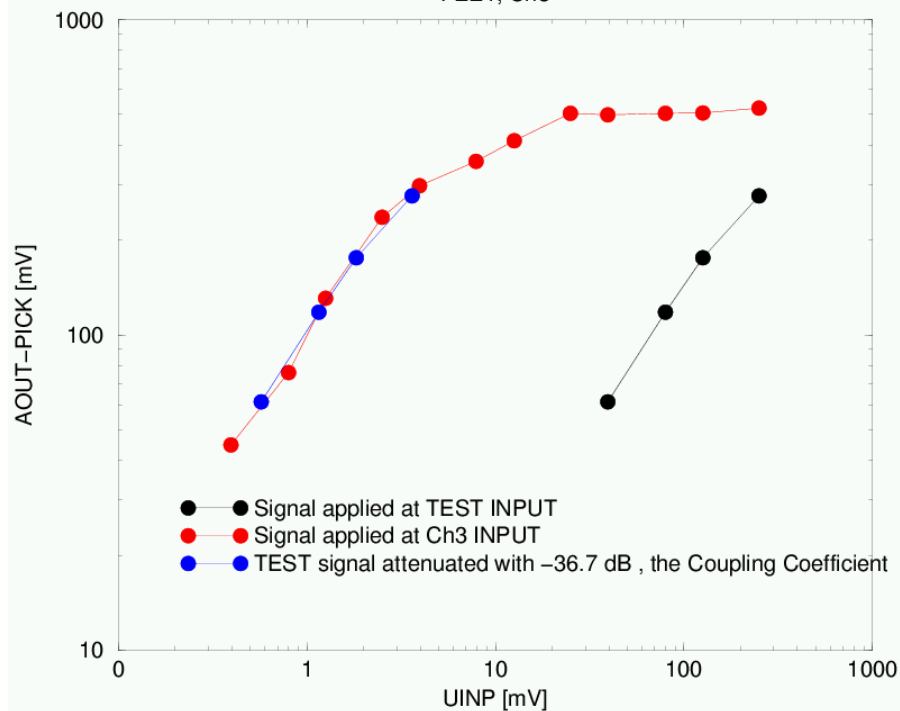
Jobname Date Designer Layouter
RPC-FEE1 1.9.2003 Ciobanu@gsi.de Ciobanu@gsi.de

Layer
Bot



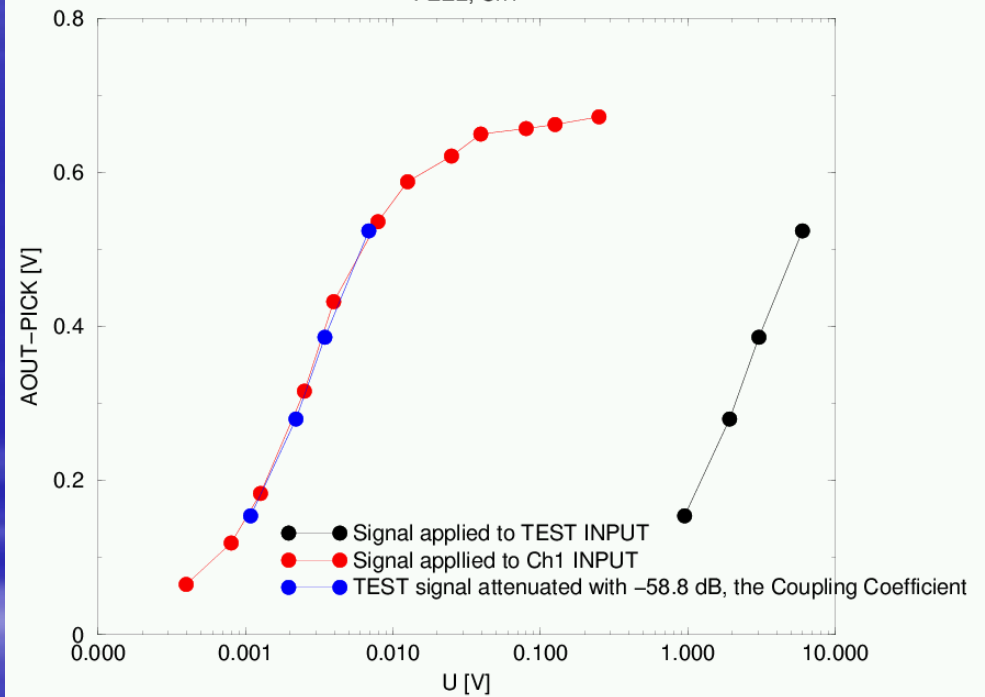
Test Line Couple Coefficient

EVALUATION of Coupling Coefficient of TEST Coupled Lines
FEE1, Ch3



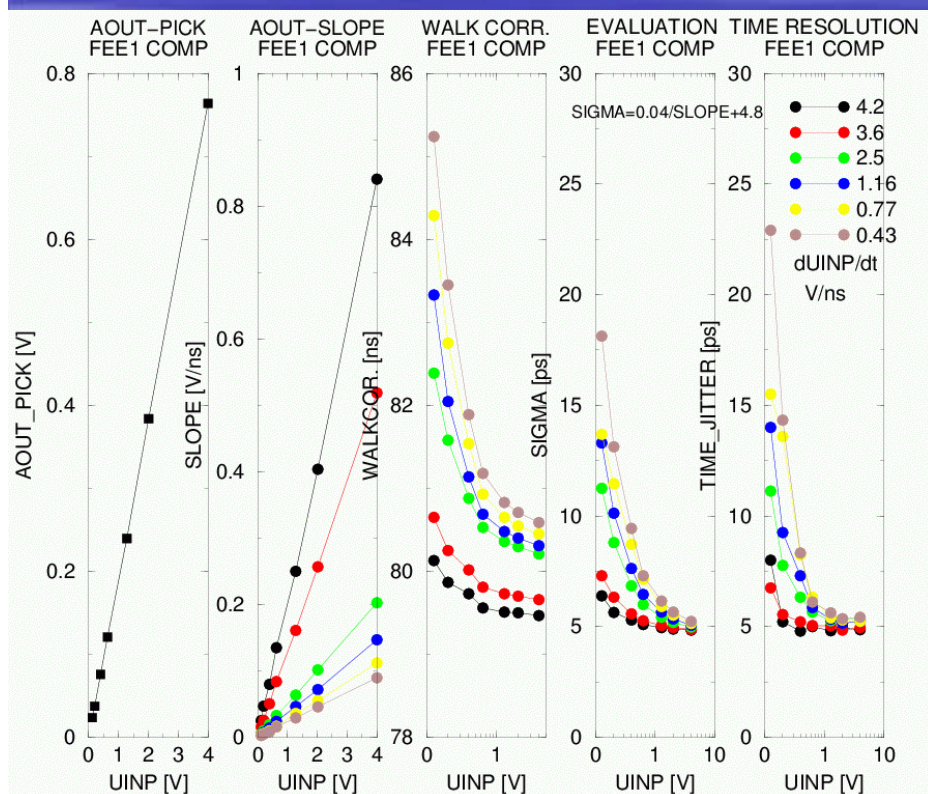
FEE1

EVALUATION of Coupling Coefficient of TEST Coupled Lines
FEE2, Ch1

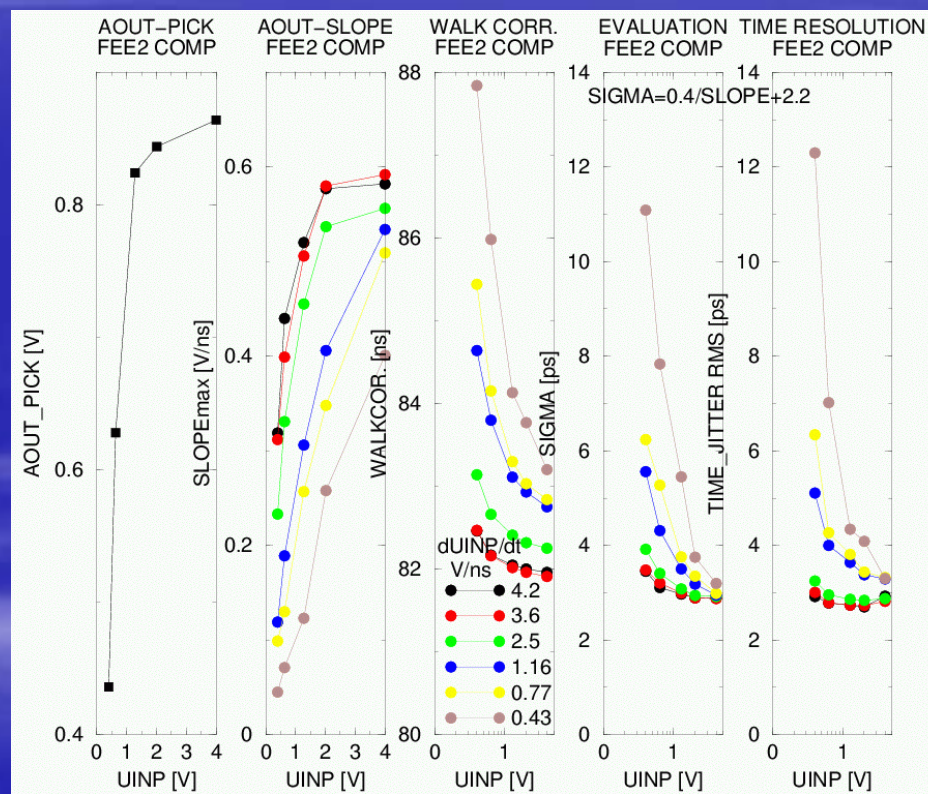


FEE2

Discriminator Timing Resolution (including the setup error)



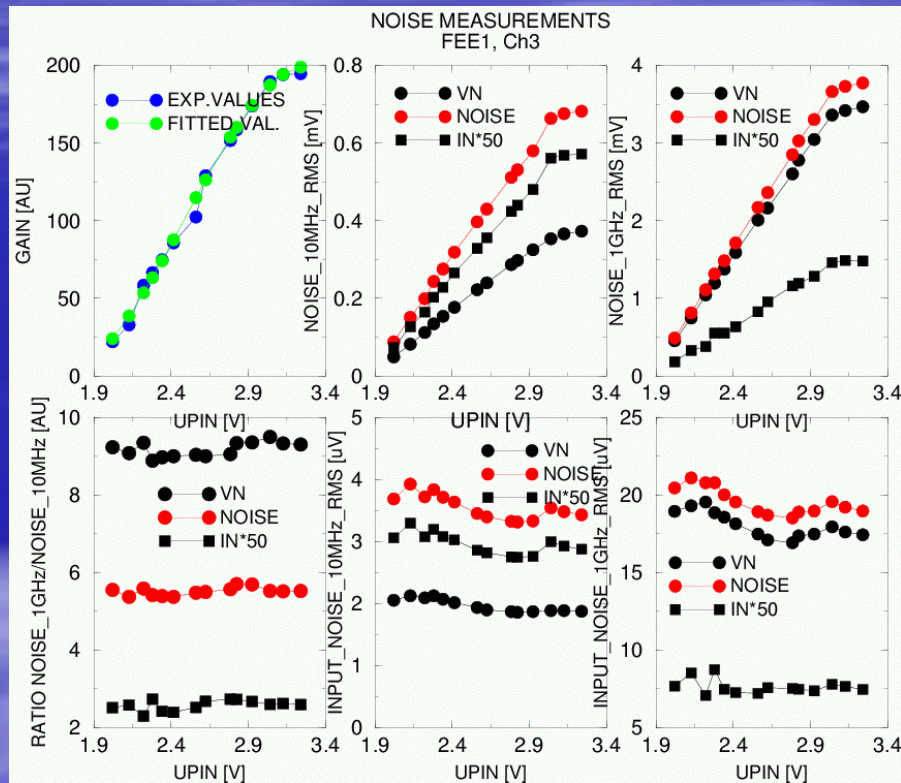
FEE1



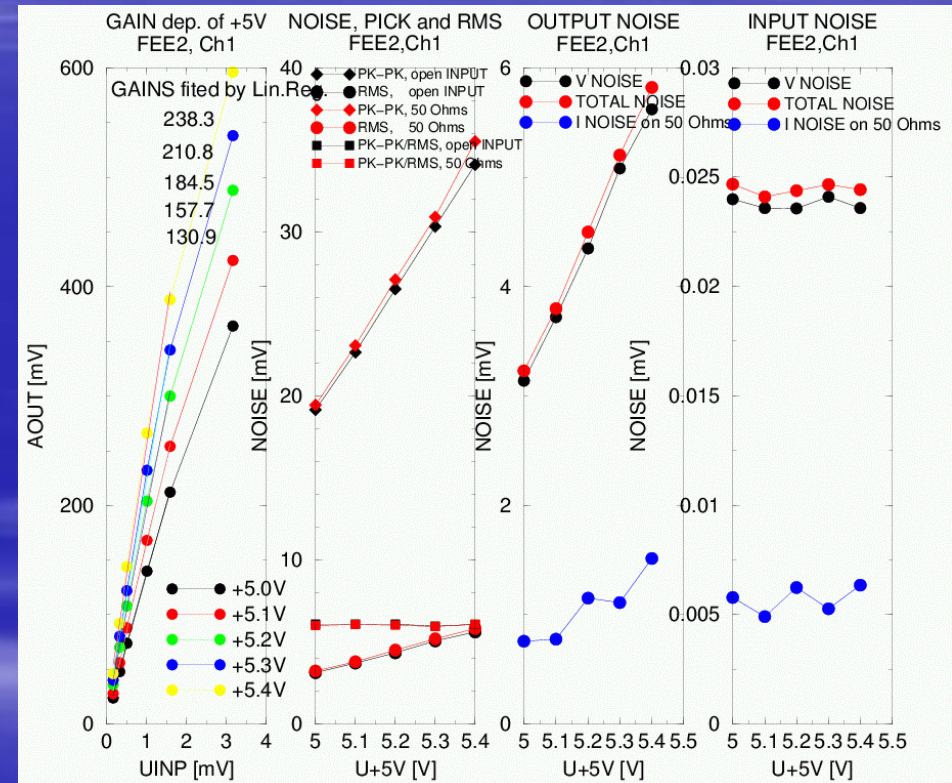
FEE2



Noise Measurements



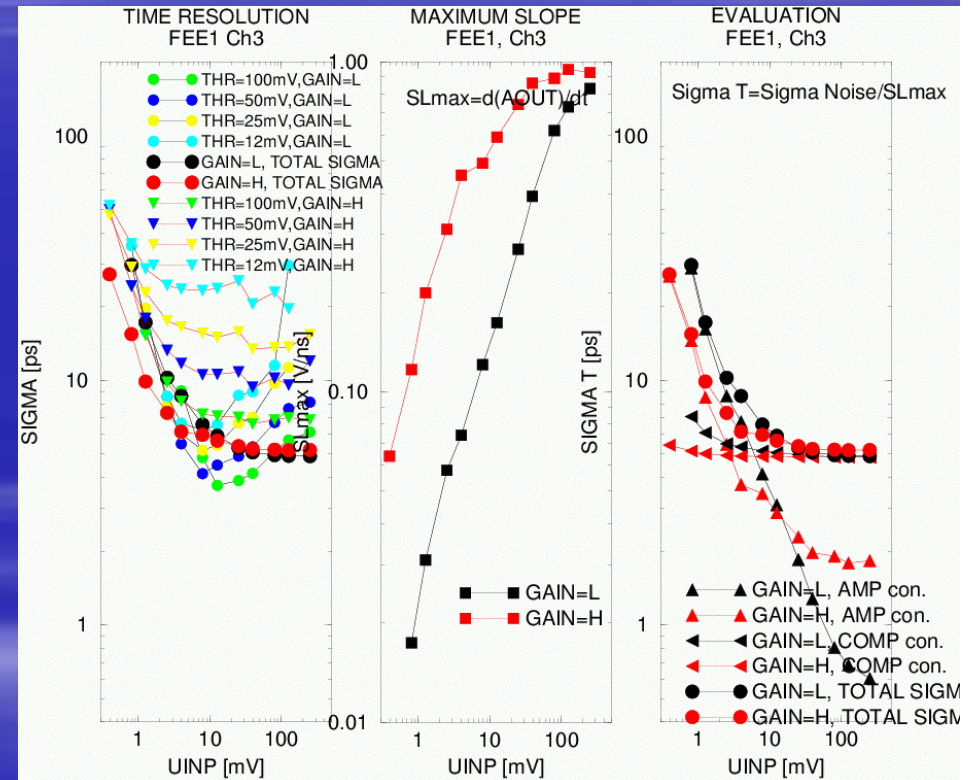
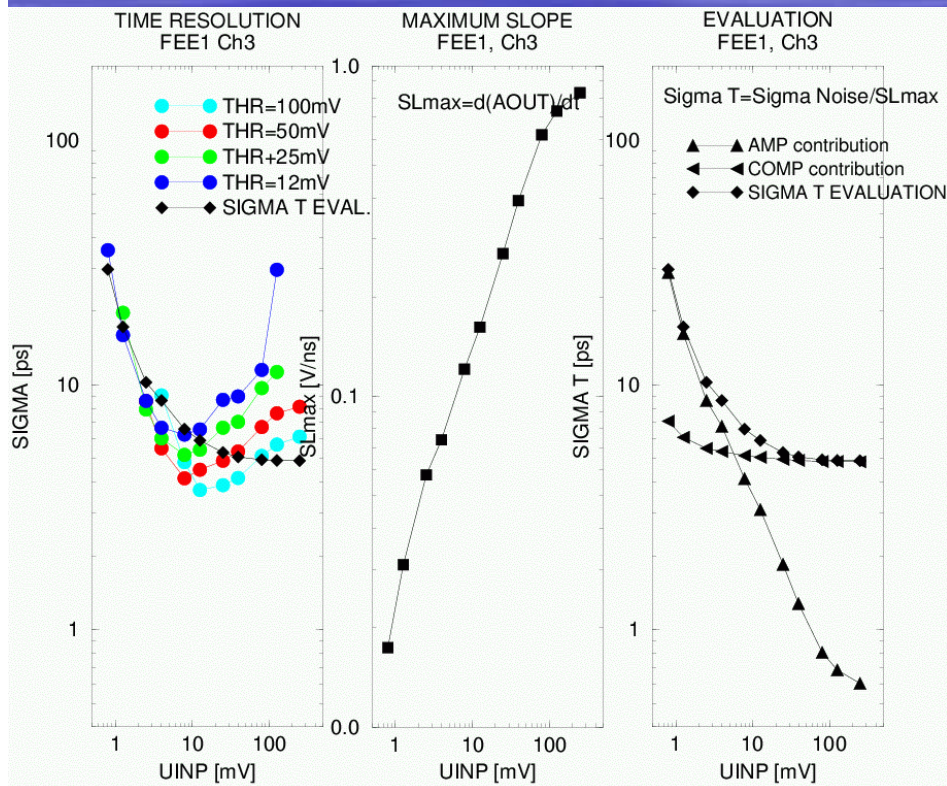
FEE1



FEE2



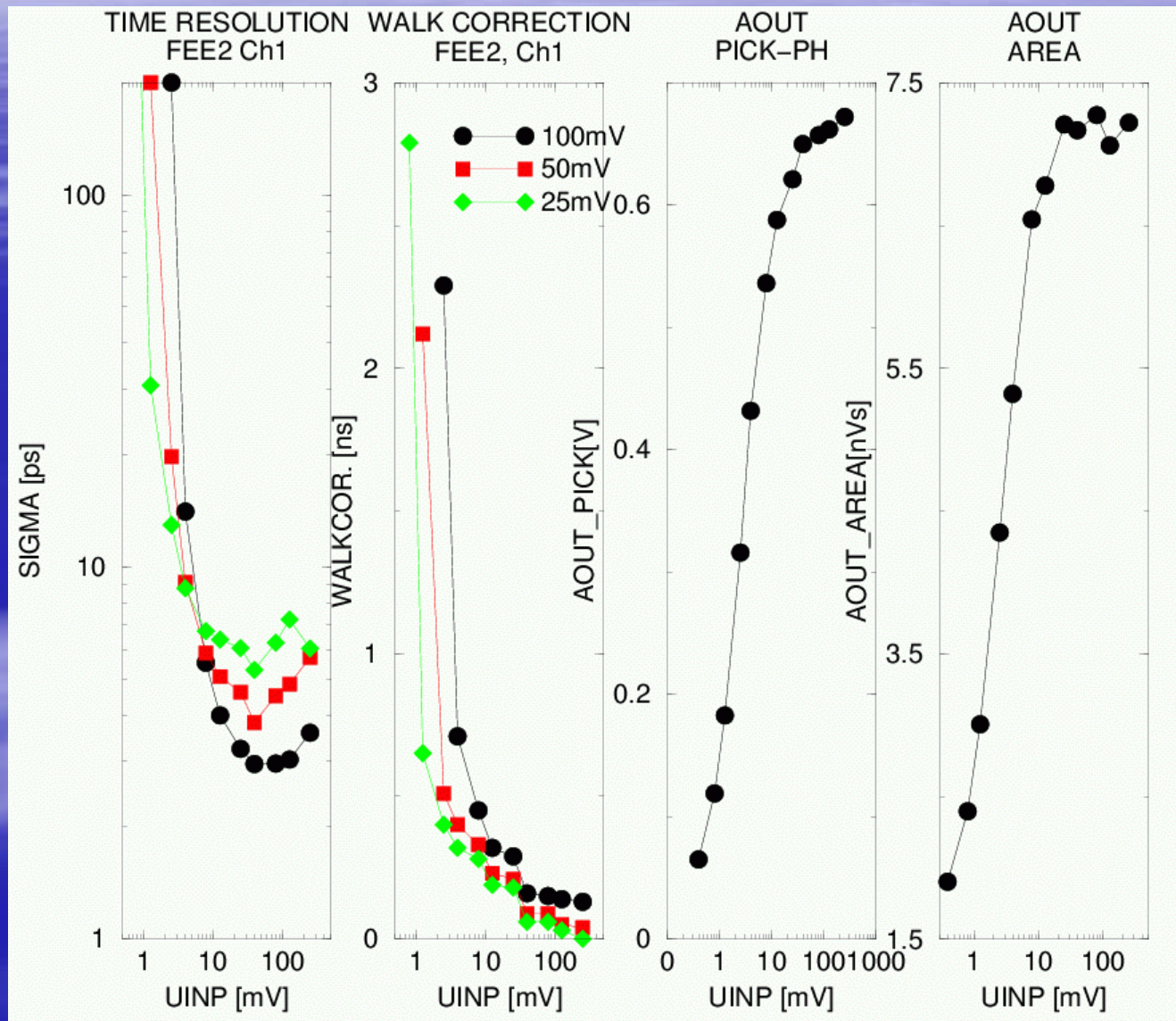
FEE1 TIME RESOLUTION



Low Gain, different Thresholds

Low and High Gain, different Thresholds

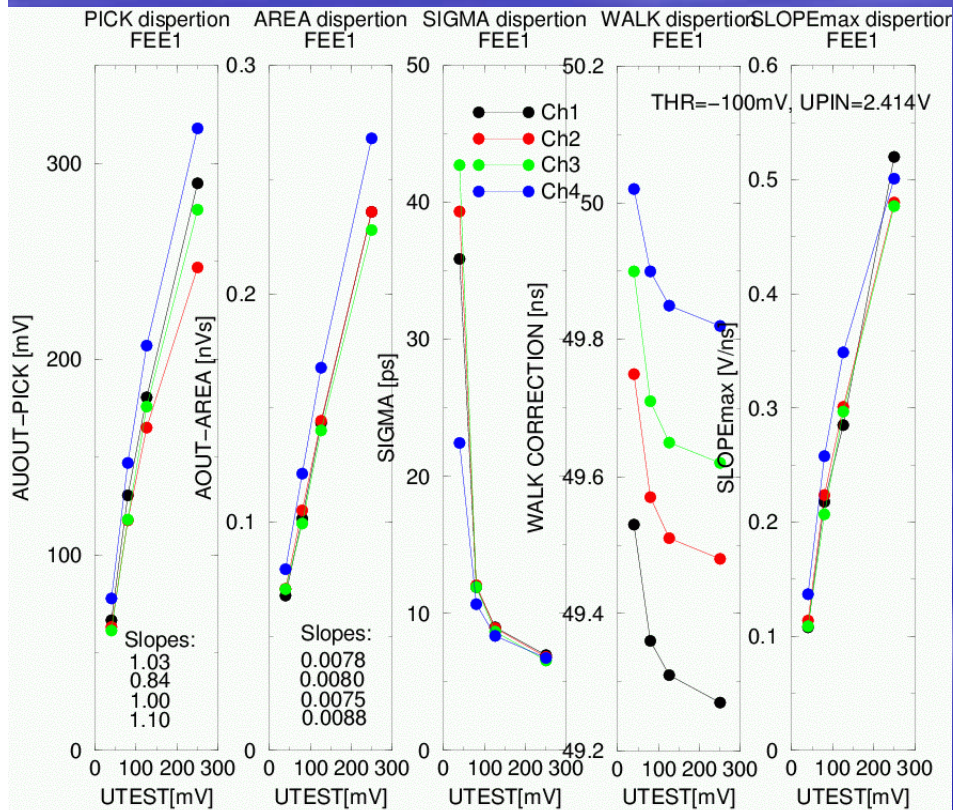
FEE2 TIME RESOLUTION



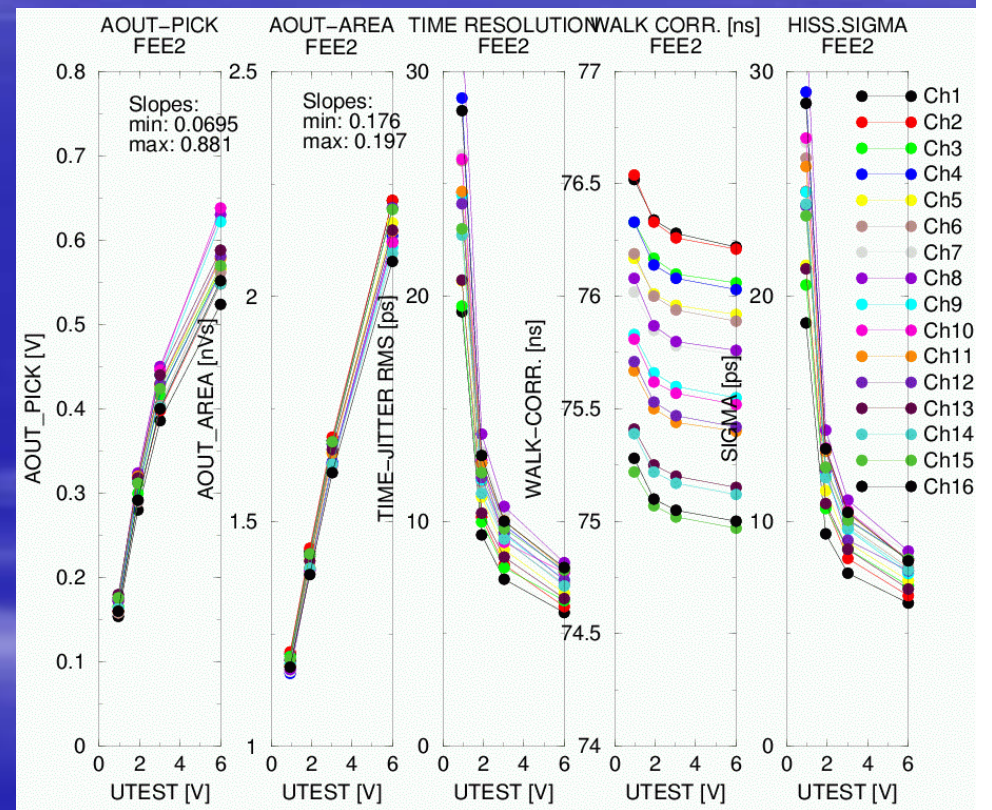
different Thresholds



Spread between channels

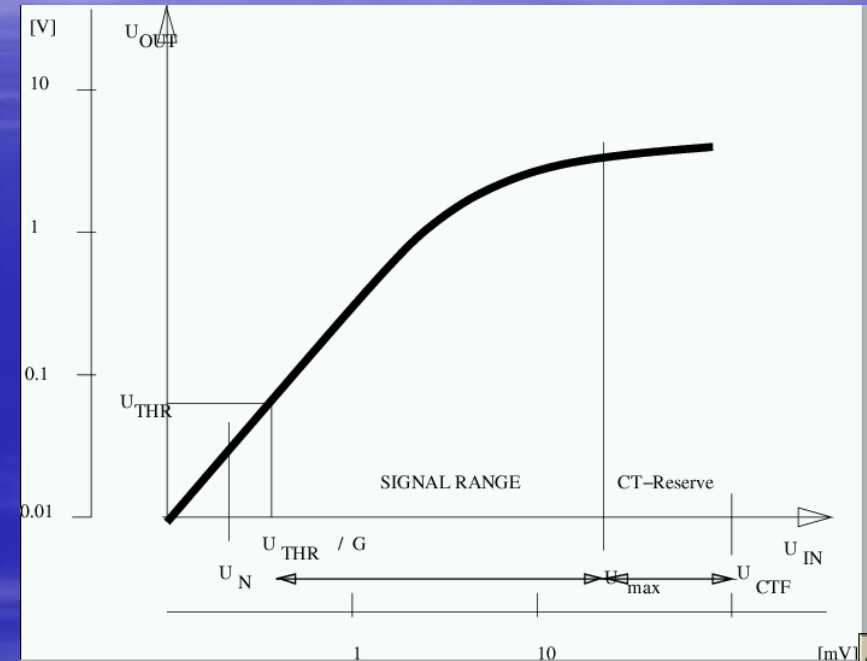
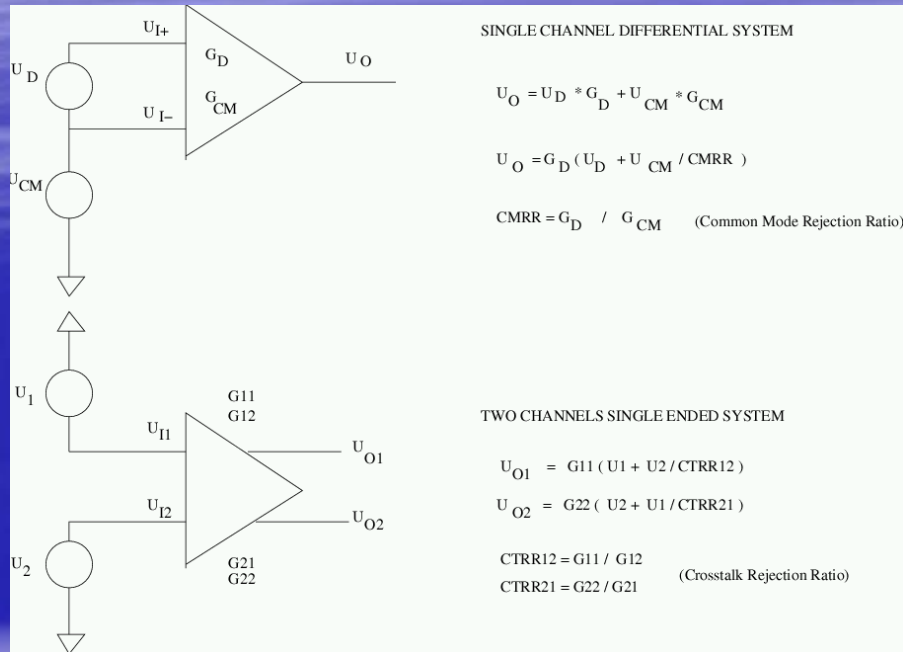


FEE1



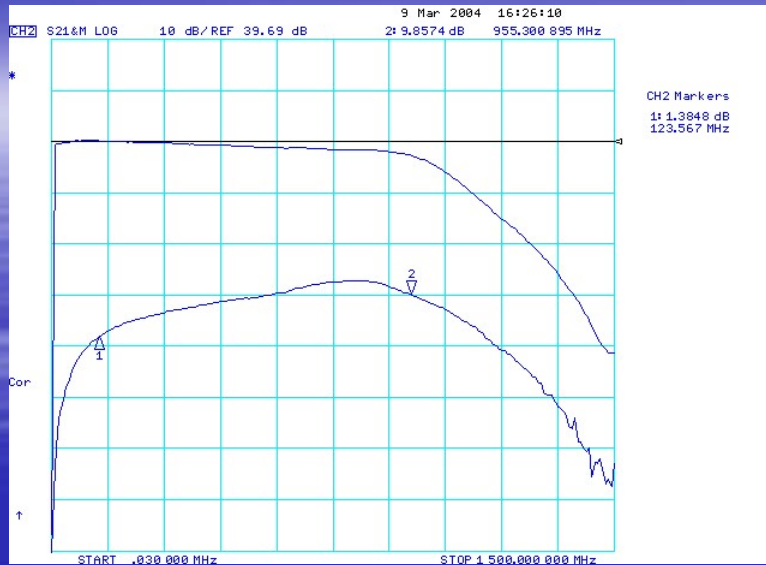
FEE2

CROSSTALK and COMMON MODE REJECTION RATIO

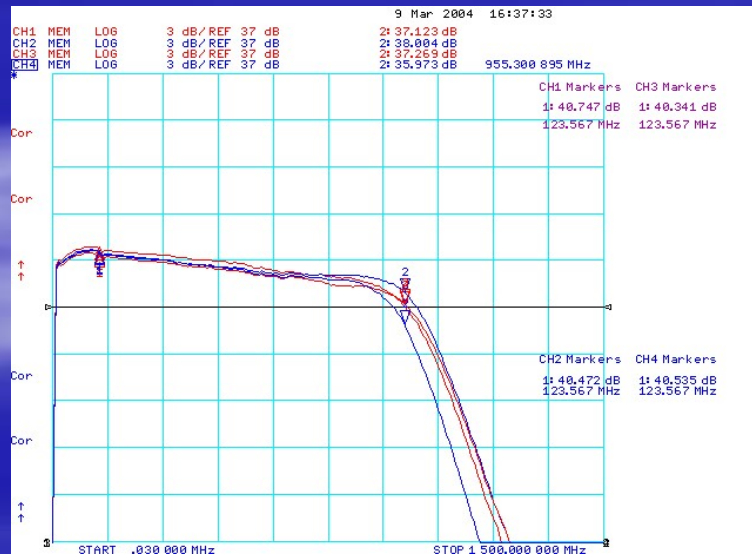


	G11	G21	G31	CTRR21	CTRR31	CMRR
				[dB]	[dB]	[dB]
FEE1	100	0.03	0.025	70.5	72	-
FEE2	-	-	-	43.8	50	-
FEE2 + Flat Cable + LEMO Adapter				39.5	45.5	-
NINO FEE	-	-	-	42.3	55.7	29.8
NINO + 50cm Twisted Pair Cable				35.5	53.7	29.8

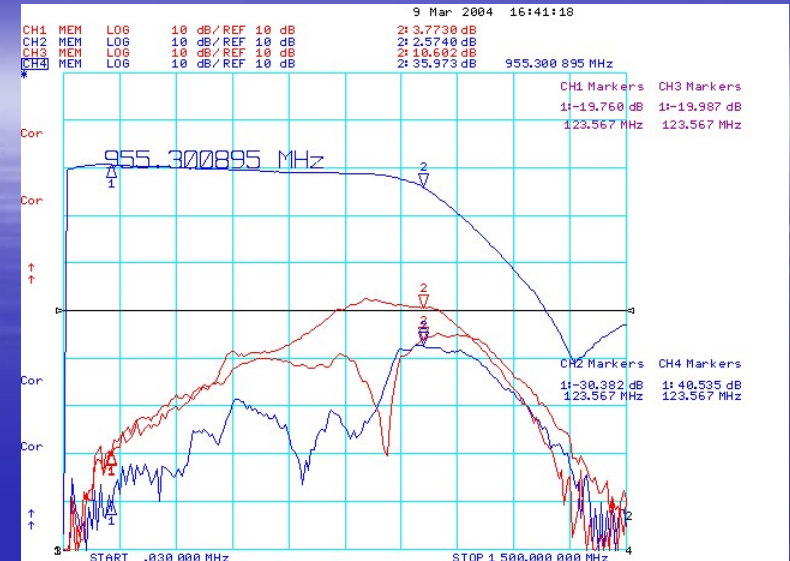
A OUTPUT Frequency Dependence



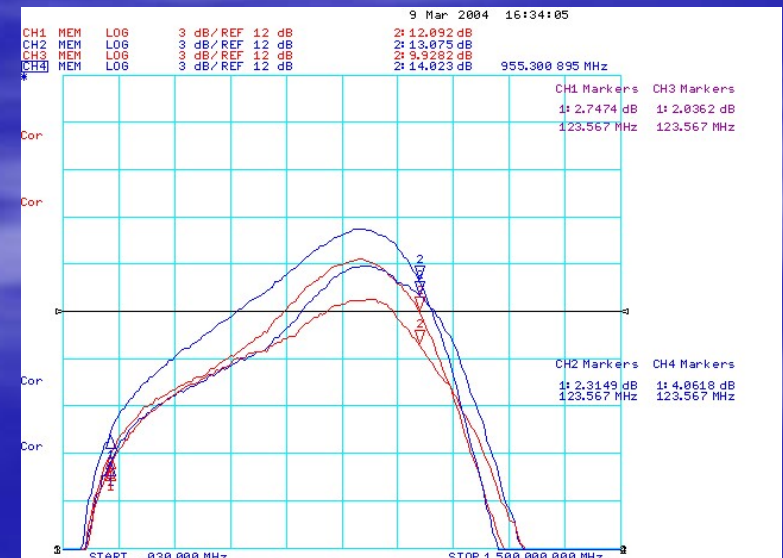
Gain Spread for 4 Channels



Crosstalk Between Channels



Gain + Couple Coefficient Spread

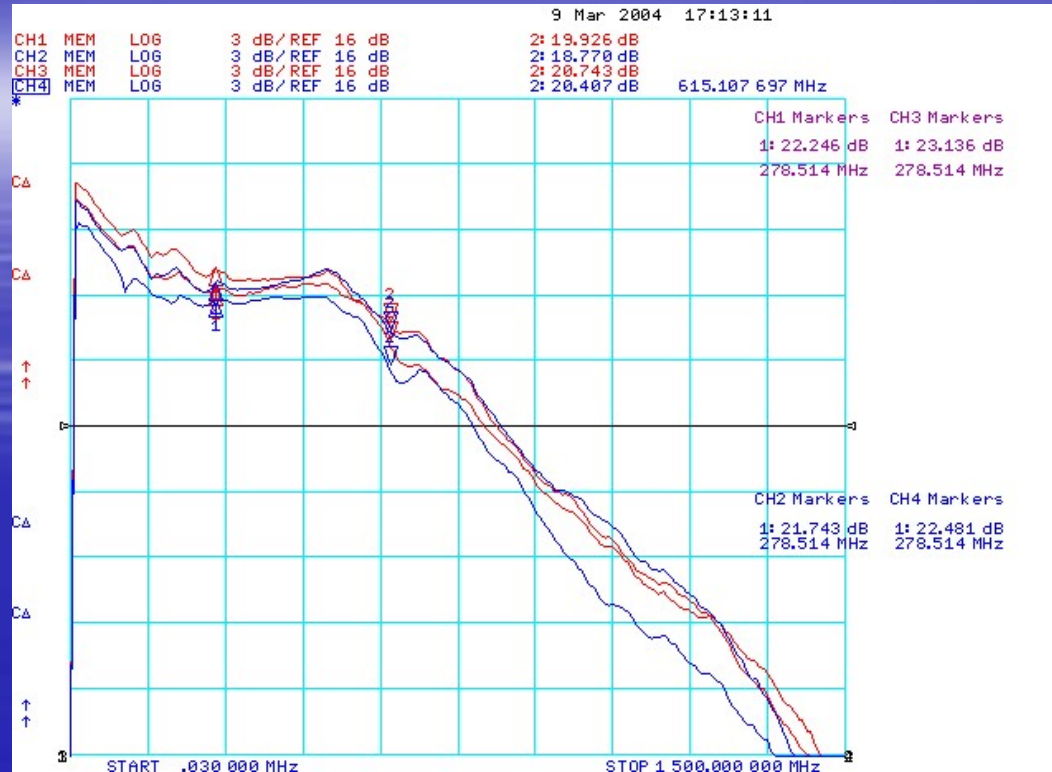


RF MEAS.
FEE1



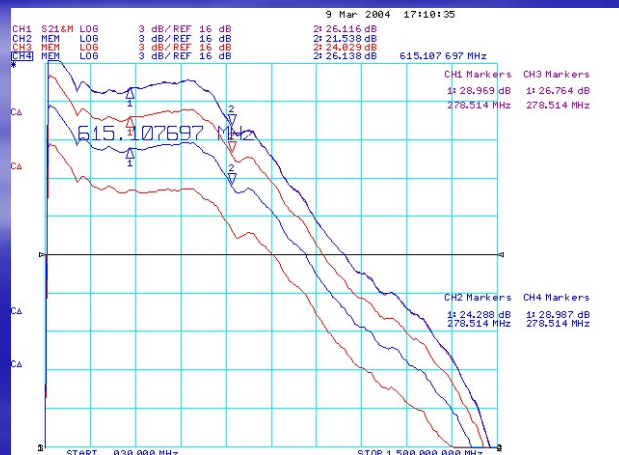
RF MEAS.
FEE2

A OUTPUT Frequency Dependence, 4 channels

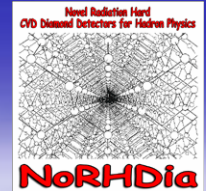


Gain Sensibility
to +5V

Test Line
Couple Coeff.

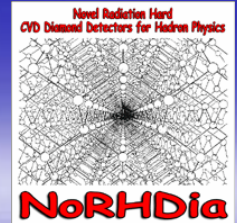


FEE Comparison (25.06.2004)



	FEE1	FEE2	NINO_FEE
1.	4 Channels	16 Channels	24 Channels
	AC Amp., LE Disc., 4*OR, THR and GAIN man. adj.	AC Amp., LE Disc., 16*OR, TEST Gen., THR software	3 * (8 Channels) Chip, 24*OR THR, HISS, ToTHR man. adj.
2.	+6V, +12V, -6V	+5V, -5V	+2.5V
	1.85 W/Channel	0.51 W/Channel	0.036 W/Channel
3. Dim.:	110mm * 95mm	149 mm * 95 mm	190mm * 100mm
4.INP.:	4 LEMO	16 Single Ended, con. MEC1	24 Diff., con. EURO
	1 LEMO TEST	ENA/DIS signal for TEST Gen. THRESHOLD Voltage	1 LEMO TEST
5.OUT.:	4 NIM for TIME	16 Diff. PECL for TIME	24 Diff. LVDS for TIME and
	4 LEMO Amplitude	16 Diff. for Amplitude	Time over Threshold
	1 LEMO OR	1 OR	1 LEMO OR
6.AC: - GAIN	~ 0-200	~160	-
- Bandwidth	~ 1GHz	~1.5GHz	-
- Noise	~ 20μV	~25μV	-
- Rise Time	~ 350ps	~250ps	-
7. Disc.:- Noise	~ 40μV	~ 400μV	-
- Rise Time	~ 500ps	~400ps	-
- Res. Jitter	~4.8ps	~2.2ps	-
8. Time Res.:	30-10-5-4-4 [ps]	128-17-11-8-6 [ps]	68-24-15-11-8 [ps]
	Preliminary measurements for Input Signal Dynamics 1 - 3 - 10 - 30 - 100 [mV]		

Some ideas for Future FEE (25.06.2004)



1. The main limitation for the use of actual design together with Diamond Detectors for MIP detection is the Signal to Noise Ratio. The Single Crystal Diamond Material is very promising if the Sensitivity of the detection can be increased.
2. To increase the Signal to Noise of FEE, the first AC cell can be replaced by a Fast Charge Sensitivity Amplifier.

CAN BE USED A PRIVATE CHIP?

3. The actual level of performances is obtained with discrete elements and the critical parts are IC top on the Market: MAXIM9601(500ps comp), GALI-S66(Advanced Silicon Techn.), DC-3GHz Amp., 2.7dB NF, 20dB Gain.
4. It is very promising the DIFFERENTIAL pick-up of the signal and the use of an 110 Ohms cheap flat cable – Major Changes in Input stage of FEE.
5. Very attractive and effective: The test of NINO chip for ToF-ALICE.